Thin-Film Transistors: Device Structures, Materials, Physics, and Applications
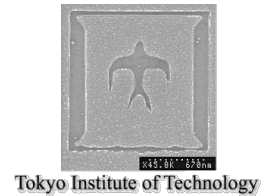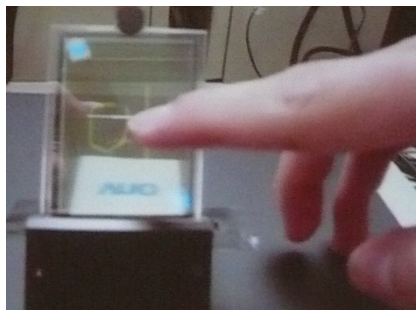
Toshio Kamiya
Tokyo Institute of Technology

Tokyo Institute of Technology

6.5" Flexible OLED 160×272, WQVGA (SMD, SID2010/APL2009)

2.4" QVGA T-AMOLED with Touch, 320×240 (AUO, SID2010, #11-2)

70" 3D AMLCD 3,840×2,160, UD (SEC, FPDI2010)

32" AM-OLED 1,920×1,080, FHD (AUO FPDI2011)

Reviews

- Keisuke Ide, Kenji Nomura, Hideo Hosono, and Toshio Kamiya
  Electronic Defects in Amorphous Oxide Semiconductors : A Review
  Phys. Status Solidi A 216 [5] (2019) 1800372-1 – 28
- T. Kamiya, H. Hosono
  Chap. Oxide TFT,
  Handbook of Visual Display Technology 2nd Ed. (Springer, 2016)
- Toshio Kamiya and Hideo Hosono
  Chap. 13 Amorphous In-Ga-Zn-O thin film transistors: fabrication and properties
  Handbook of Zinc Oxide and Related Materials
  (Taylor & Francis, 2012)
  Toshio Kamiya, Kenji Nomura and Hideo Hosono
- *Present status of amorphous InGaZnO thin-film transistors*
  Sci. Technol. Adv. Mater. 11 (2010) 044305
- Toshio Kamiya and Hideo Hosono
  Material characteristics and applications of transparent amorphous oxide semiconductors
  NPG Asia Mater. 2 (2010) 1522
- Toshio Kamiya, Kenji Nomura, and Hideo Hosono
  Origins of high mobility and low operation voltage of amorphous oxide TFTs:
  Electronic structure, electron transport, defects and doping
  IEEE J. Display Technol. 5 (2009) 273

CONTENTS

Types of transistors

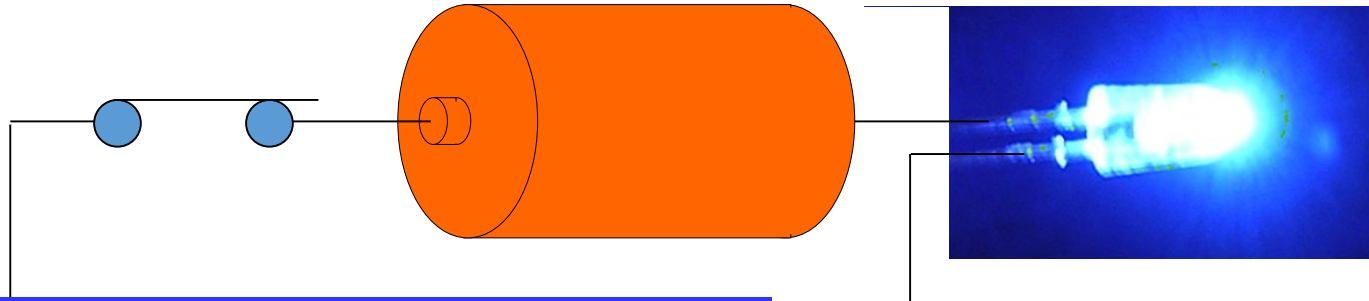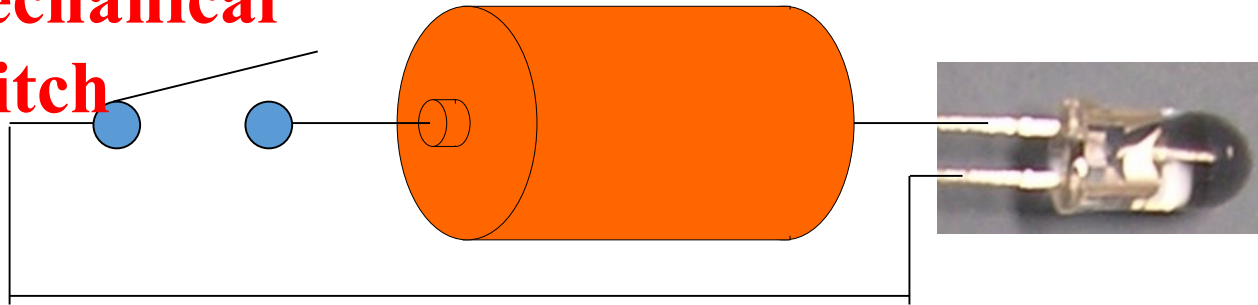## 1. Bipolar transistors
* n/p/n, p/n/p junction transistors

2. Field-effect transistors (FET)
* Metal-Oxide (SiO_2) -Silicon (MOS) FET
* Metal-Insulator-Semiconductor (MIS) FET
* Thin-Film transistor (TFT)
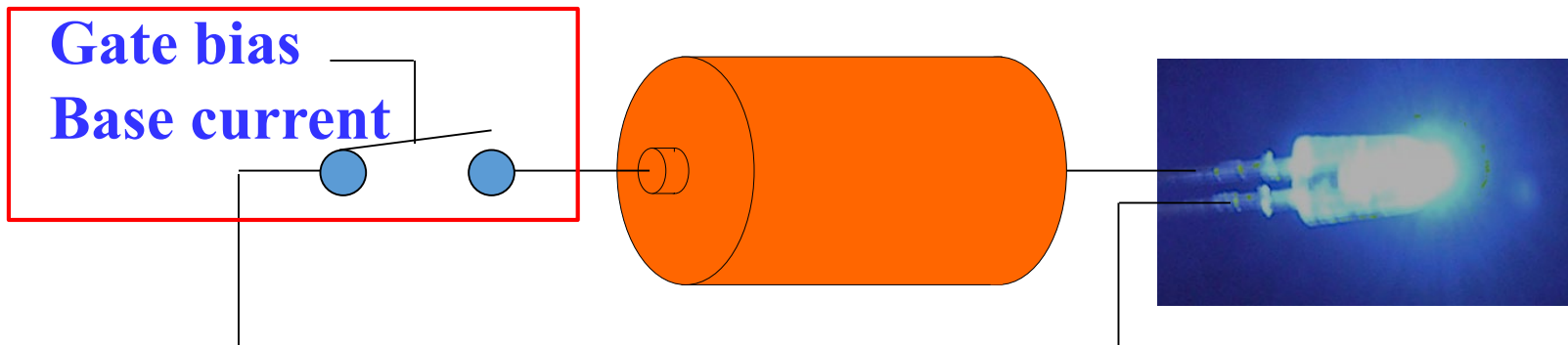* Single-electron tunneling transistor (SETT)

Transfer resistance: Transistor
A switch controllable by electric signal
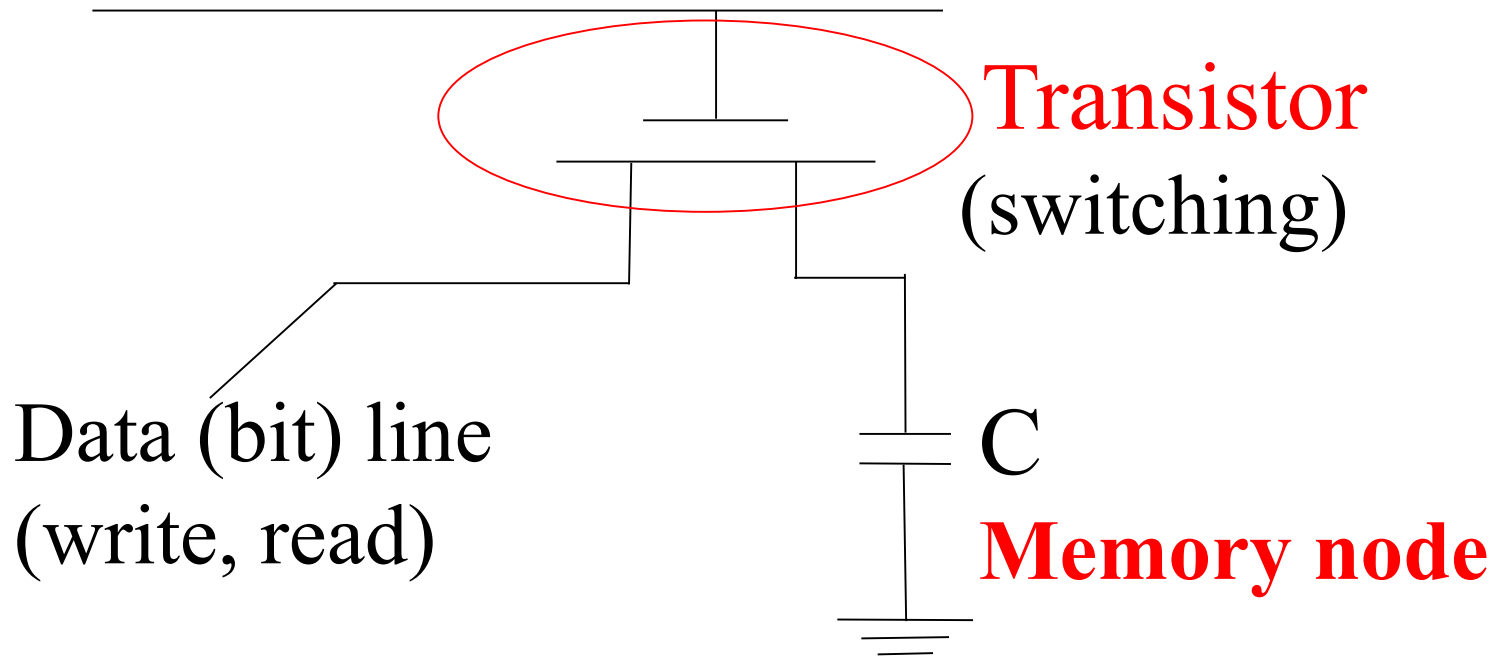
Mechanical switch

Transistor: 3-terminal device

Gate bias
Base current

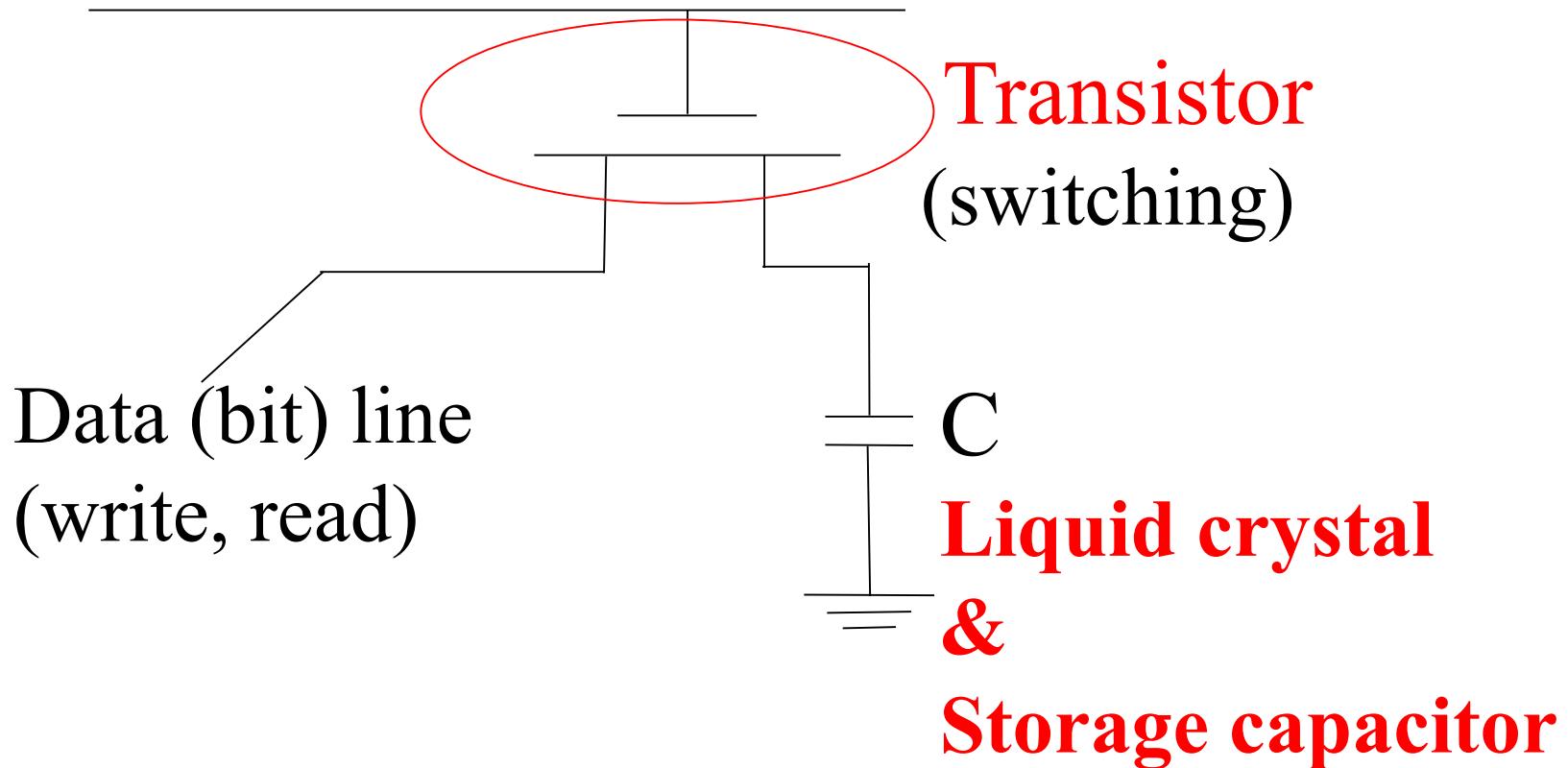# Transistor (switch) can build a computer

e.g., Memory circuit

Word line (write)

Transistor
(switching)

Data (bit) line
(write, read)

C

Memory node

Transistor (switch) can build a computer

e.g., Display pixel

Word line (write)

Data (bit) line
(write, read)

Transistor
(switching)

C

Liquid crystal
&
Storage capacitor
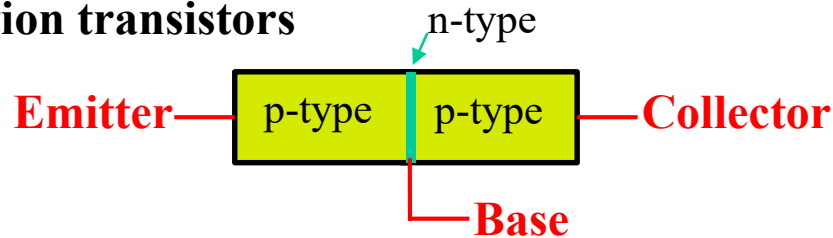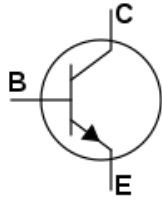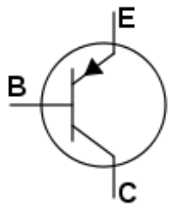
Bipolar vs Unipolar transistors

Bipolar transistor: Both electrons and holes contribute to device operation
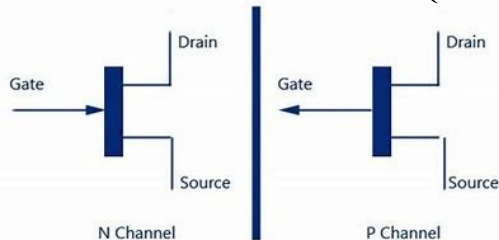
-      p/n/p,   n/p/n junction transistors

n-type

Emitter —— | p-type | p-type | —— Collector

Base

   * Carrier flows a small electrode distance (E – C),
     high-density current possible.

   * $I_{E\text{-}C}$ is controlled by **the base current I_B**, difficult to reduce I_B
     => **Rather high power consumption, not suitable for CPU, Memory, Display …**

Unipolar transistor: Either of electrons or holes contribute to device operation

- **Field-effect transistor (FET)**

Drain   Drain
Gate   Gate
Source   Source
N Channel   P Channel

Source   Drain
Semiconductor (any of *n, i, p*)
Gate insulator
Gate

   * Carrier flows a long distance (S – D),
     current density limited
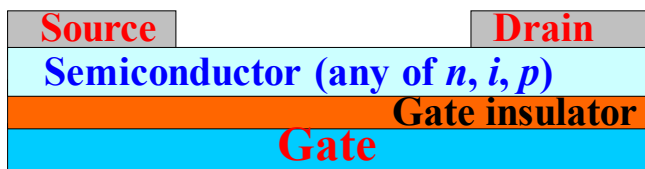
   * I_{SD} is controlled by the gate voltage V_G,
     I_G is reduced by the resistance of gate insulator

   => **Low power consumption at off states,
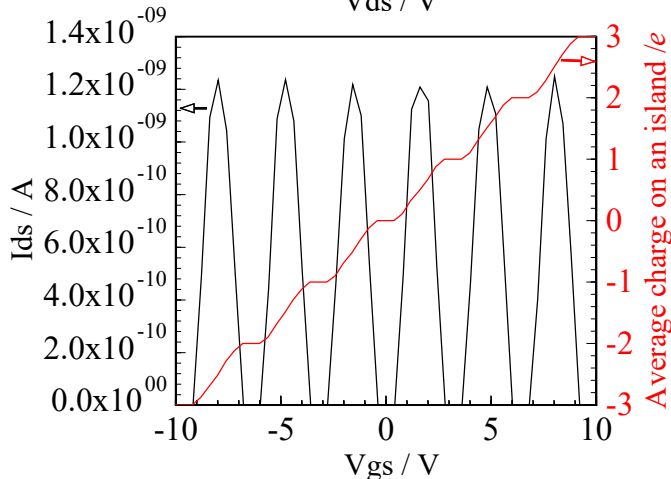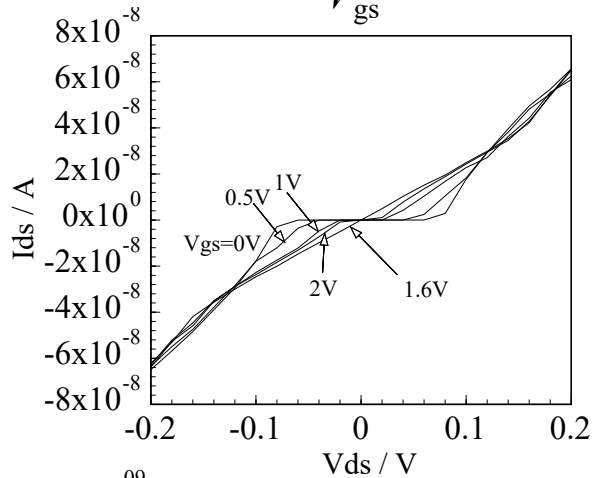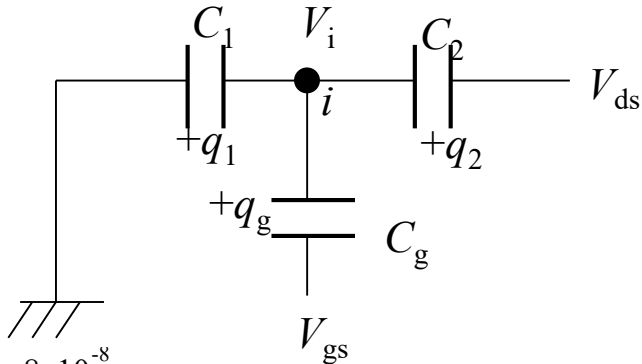   used for CPU, Memory, Display**

     * **Metal-Oxide (SiO_2) -Silicon (MOS) FET**
     * **Metal-Insulator-Semiconductor (MIS) FET**
     * **Thin-Film Transistor (TFT)**

Single-electron tunnel transistor (SETT)

Composed of:
1. **Very small charging island**
2. **Electrons are confined by three insulators, C_1, C_2, and C_g**
3. **Electrons pass through C1 and C2 by tunneling**
4. **Electrons behave as particles if R_{C1} and R_{C2} >> quantum resistance**

1. **Electrons behave as particles if R_{C1} and R_{C2} >> quantum resistance $h/e^2 = 26k\Omega$**
2. **Operation voltage (e.g., Coulomb gap $\Delta V_{ds} = 2e/C_{\Sigma}$) is limited by the total capacitance $C_{\Sigma} = C_1 + C_2 + C_g$**
3. **Very small $C_{\Sigma} \sim aF$ is required for room temperature operation (e.g., cross-section area < 3x3 nm^2)**
4. **Operation characteristic is changed very largely by the number of electrons confined in the charging island => Very low power consumption**
5. **Operation speed is limited by R_C**
6. **Very small power consumption**
7. **Combination of SETT is used for ultimately low power consumption memory, quantum computer node, etc**

SETT memory in very thin nc-Si
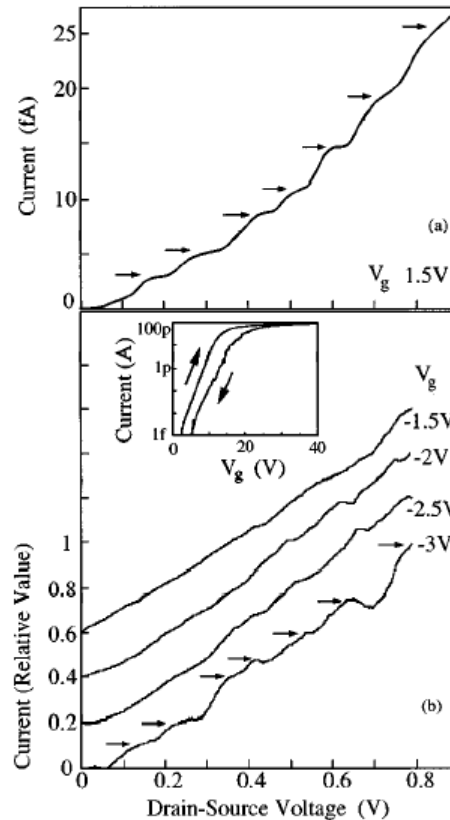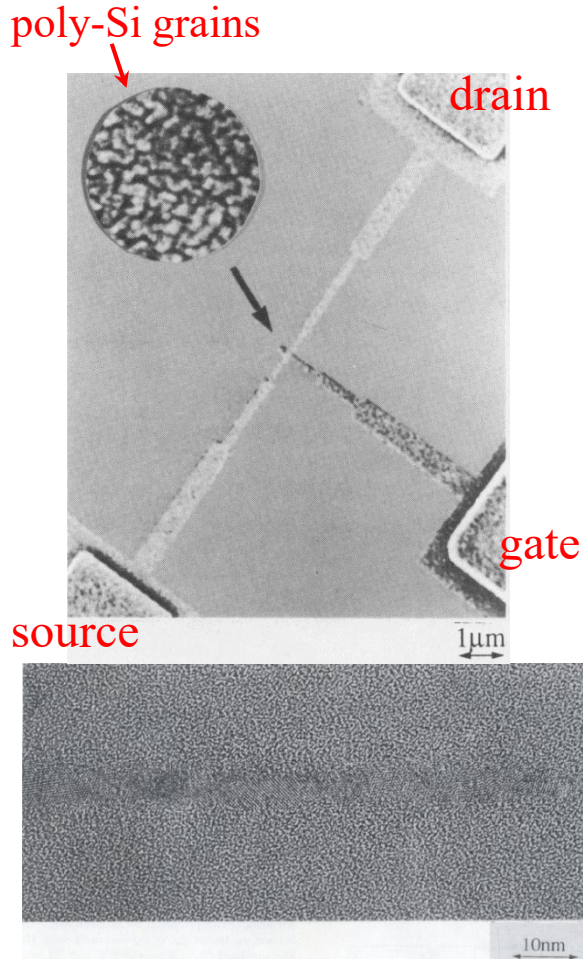

poly-Si grains

drain

gate

source

1μm

10nm

FIG. 2. Measured current vs drain-source voltage at room temperature. The top panel shows the result of the first run. The bottom panel is the data for same sample measured on a different day with various gate voltages. The vertical axis is the relative value, which is measured current divided by the current at 0.8 V. Because the threshold voltage of the sample had become lower in the latter, the gate voltage was adjusted to have the similar current as the former. The inset is the measured current vs gate voltage. The gate voltage is swept from 0 up to 40 V, and then swept down to 0 V. The sweep rate is 0.02 V/s. The drain-source voltage is 10 mV.
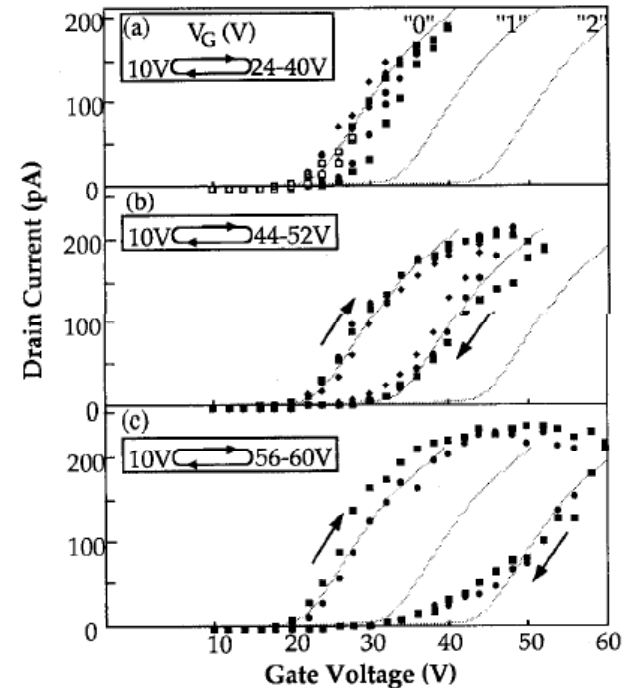

Fig. 12. Measured drain current versus gate voltage. The drain-source voltage is 50 mV. The gate-voltage sweep rate is 4 V/min. The maximum gate voltage in a sweep loop is 24 V (○), 28 V (□), 32 V (◇), 36 V (●), 40 V (□) in (a), 44 V (◇), 48 V (●), 52 V (□) in (b), 56 V (●), and 60 V (□) in (c).

K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai and K. Seki: *Room-temperature single-electron memory*; IEEE Trans. Electr. Dev. **41** (1994) 1628.

K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai and K. Seki: *Transport characteristics of polycrystalline silicon wire influenced by single-electron chargin at room temperature*; Appl. Phys. Lett. **67** (1995) 828.

CONTENTS

Typical structures of FETs

n-ch MOS FET

n channel   n+ c-Si contact

p^- c-Si

Substrate bias

n-ch a-Si:H / a-IGZO TFT
Inverted staggered structure

i a-Si:H   n+ a-Si:H contact

Insulating substrate (glass)

n-ch poly-Si / a-IGZO TFT (high speed)
Co-planar / self-aligned structure

i poly-Si   n+ poly-Si contact

Insulating substrate (glass)

n-ch oxide TFT for research purpose
top-contact, top-gate structure (staggered structure)

n^- oxide semiconductor

metal contact

Insulating substrate

ITO   ITO

Y_2O_x ITO

a-InGaZnO$_4$

PET

Typical AOS TFT structures

Top gate, top contact

Gate insulator
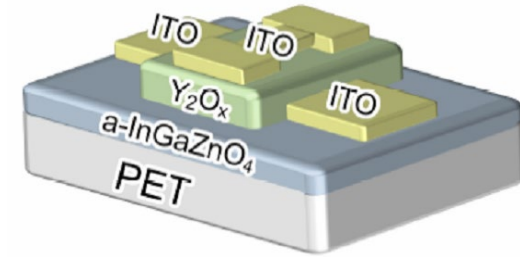
metal gate

metal source · metal drain

Semiconductor

SiO$_2$ · Insulating substrate

ITO · ITO · ITO
Y$_2$O$_x$
a-InGaZnO$_4$
PET

Top gate, bottom contact

metal gate · Gate insulator

metal source · metal drain

Semiconductor

SiO$_2$ · Insulating substrate

Bottom gate, top contact

metal source · metal drain

Semiconductor
SiO$_2$

n$^+$ Si

Inverted Staggered · Semiconductor
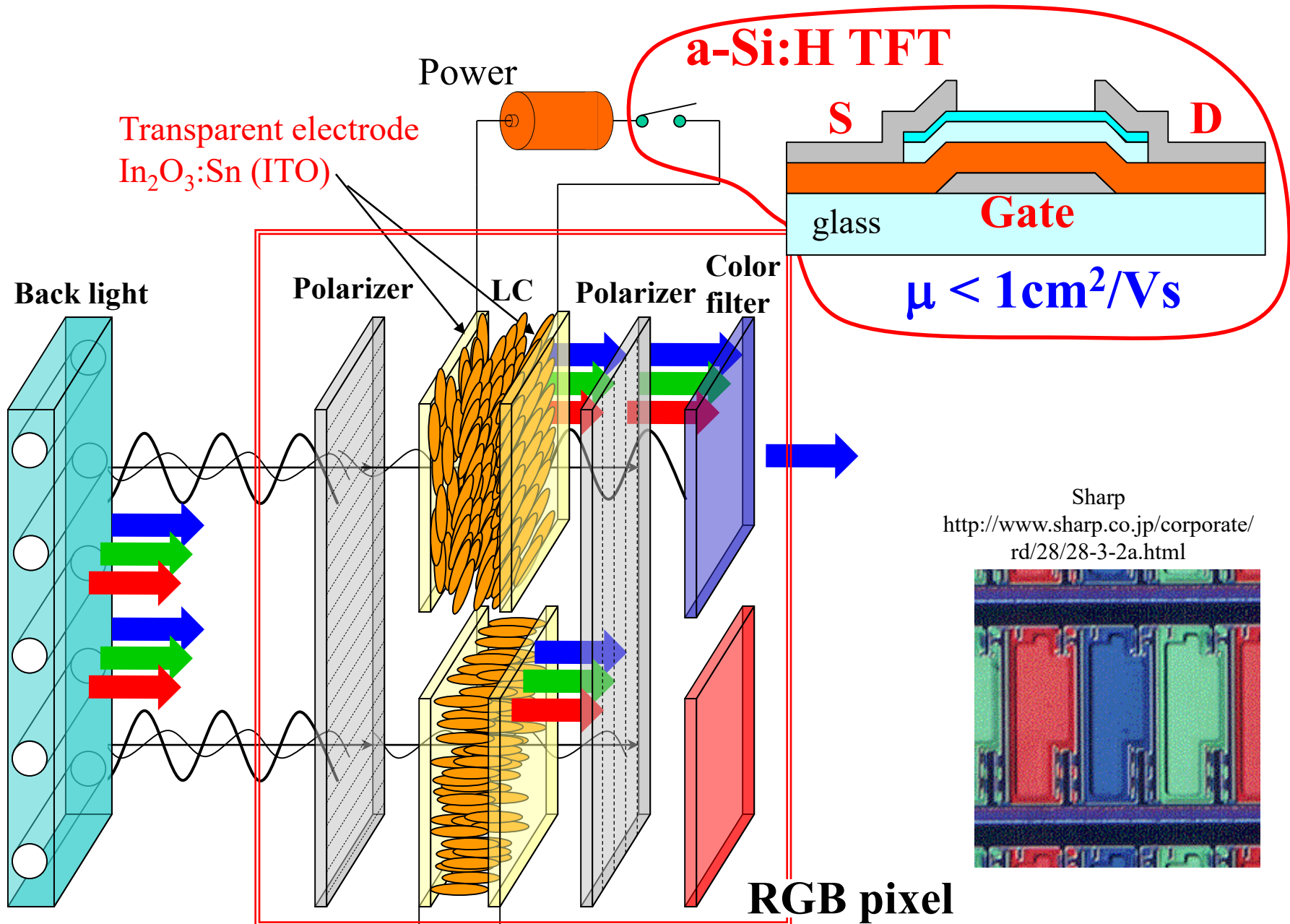
a-SiN$_x$

SiO$_2$

Insulating substrate: glass, SiO$_2$/Si etc.

Semiconductor: a-In-Ga-Zn-Sn-O

Gate insulator: SiO$_2$, SiON, Al$_2$O$_3$, Y$_2$O$_3$, HfO$_2$, CaHfO$_3$, ATO (Al$_2$O$_3$/TiO$_2$) etc.

Metal: Au, Ti, Al, ITO etc., n$^+$-ZnO, n$^+$-IGZO, n$^+$-IZO buffer layers etc

TFT application: Active Matrix LCD

a-Si:H TFT

Power

Transparent electrode
In$_2$O$_3$:Sn (ITO)

S   **D**

glass   **Gate**

$\mu < 1\,cm^2/Vs$

Back light   **Polarizer**   **LC**   **Polarizer**   **Color filter**

RGB pixel
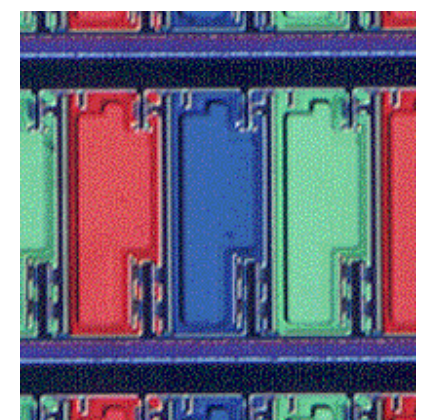
TFT channel materials

	Amorphous oxide	a-Si:H	LTPS	HTPS	µc-Si:H	Organic
Mobility	**6-20 (100?)**	< 1	30 – >100	30 – >100	< 10	**<< 1**
Fast operation	○	×	◎	◎	△	×
Channel	**N-ch**	N-ch	CMOS	CMOS	CMOS	CMOS
Integration	○	×	◎	◎	△	×
Uniformity	◎	◎	×	△	△	◎?
Stability	△	×	◎	○	○	**?**
Process T	**RT-600ºC**	150-350ºC	~400ºC	>500ºC	<350ºC	RT
Solution/Printing	△	×	×	×	×	◎
TFT mask steps	**4-5 / 6-7**	4-5 / 6-7	5-9	5-9		
Pixel circuit	**2T1C**	4T2C	5T2C			
Cost/Yield	○/◎	◎/◎	×/×	×/×	○/○	
Glass size generation	**G8 (G10.5)**	≥ G10	G4	G8	G10 ?	
Display mode	**LCD, OLED, E-paper**	LCD, E-paper	LCD, OLED	LCD, OLED	LCD, OLED, E-paper	E-paper
Substrate	**Glass, metal, plastic**	Glass, metal, plastic	Glass, metal	Glass, metal	Glass, metal	Glass, metal, plastic
Issue	**Maturity Sensitivity**	Stability	Uniformity Laser Cost	Uniformity	I_{off} Mobility Uniformity	Maturity Stability

LTPS: Poly-Si crystallized by laser anneal   HTPS: Poly-Si crystallized by high-temperature anneal

a-Si:H: amorphous Si deposited by PECVD   µc-Si:H: microcrystalline Si deposited by PECVD

Channel fabrication method

1. **Si MOS FET**
   Channel: Lightly-doped single-crystal Si substrate

2. **a-Si:H TFT**
   Channel: Plasma-enhanced CVD (PECVD) using SiH_4 source gas

3. **Low-temperature poly-Si (LTPS) TFT**
   Channel: Laser-crystallized poly-Si (Laser annealing)

4. **High-temperature poly-Si (HTPS) TFT**
   Channel: Thermmaly-crystallized poly-Si
   MIC (Metal-induced crystallization)

5. **Organic TFT**
   Channel: Mainly by solution / printing method
   Evaporation is used for small molecules

6. **Oxide TFT**
   Channel: Sputtering for commercial product
   PLD, mist CVD, solution process etc are used for research

Production processes of TFT/LCD

	a-Si TFT (Matsushita)*	5 masks a-Si TFT*	4 masks a-Si TFT*	IGZO (SMD, IMID2009)	4 masks IGZO (Brother, IDW'08)
1	1st ITO (ITO)	Gate (metal)	Gate	GM depo./pattern	S/D depo.(SAM)/pattern
2	2nd ITO (SiO_2/ITO etch)	Channel (SiN_x/a-Si/n^+)	S/D/Channel	Active dep., W/E	(Channel/**Inkjet**/Etch)
3	Pixel contact (SiO_2 etch)	S/D (metal)	Passivation/ G.I.	C/H, ESL, Via pattern	GM/Insulator/channel Self-align etch to channel
4	Scan line ($Cr/MoSi_2$)	Passivation (SiN_x)	Pixel	S/D patterning	Inter layer/Via hole
5	Etch stopper (SiN_x/a-Si/SiN_x)	Pixel electrode (ITO)		Passivation patterning	Pixel electrode
6	Channel (n^+/a-Si)			Anode patterning (for OLED)	
7	Contact (SiN_x etch)			Pixel define	
8	Contact $MoSi_2Al$				

Typical process flow for a-IGZO TFT
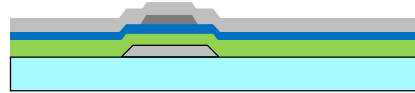
gate metal

substrate
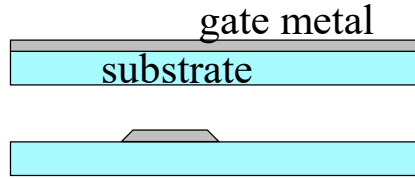
I. Gate depo (Mo/Ta/W/Al:Nd etc, sputter)
   1st PEP (Photo Engraving Process), Etching

ESL
Semi
GI
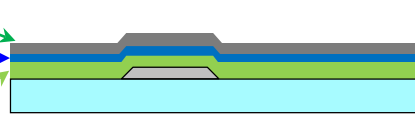
II. Gate insulator (GI), semiconductor (Semi), *(ii) Annealing of a-IGZO*
   (etch stopper layer, ESL) depo   *(iii) Plasma treatment*
   GI (ESL): $SiO_2/SiN_x/Si(O,N)$ (sputter, plasma CVD)
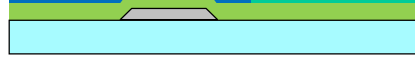   Semi: a-IGZO etc (sputter)
   2nd PEP for ESL, Etching

(iii') Plasma treatment for BC

III. Source / drain (S/D) depo (Cr/Mo etc, sputter)
   $2nd_{BCE}/3rd_{ESL}$ PEP (Etching)
   for S/D isolation, channel isolation

data line

V. Passivation layer (PL, SiO_2/SiN_x, sputter, PECVD)

(iv) Annealing

IV. $3rd_{BCE}/4th_{ESL}$ PEP, Via hole by etching

pixel el

VI. Pixel electrode (ITO etc)
   $4th_{BCE}/5th_{ESL}$ PEP, etching

G8 (> 2×2 m²) sputtering / target for IGZO

ULVAC

In-plane target (cathode & anode)
AC (20~50kHz) (/DC) sputtering
Monolithic target
Moving cathode

Pre-sputtering area → glass

Moving cathode
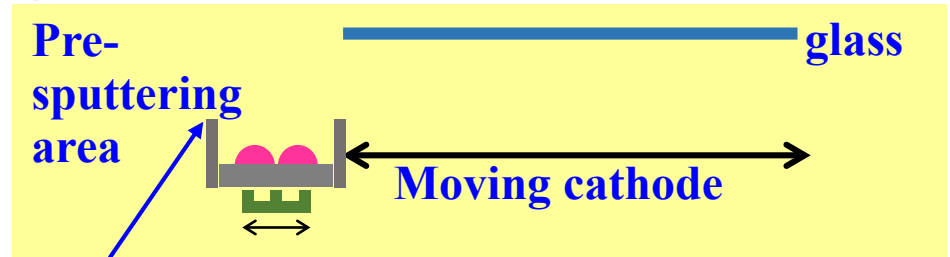
Control direction of impinging precursors

Nippon Mining & Metals

次世代TFT半導体材料　IGZO

日鉱金属株式□
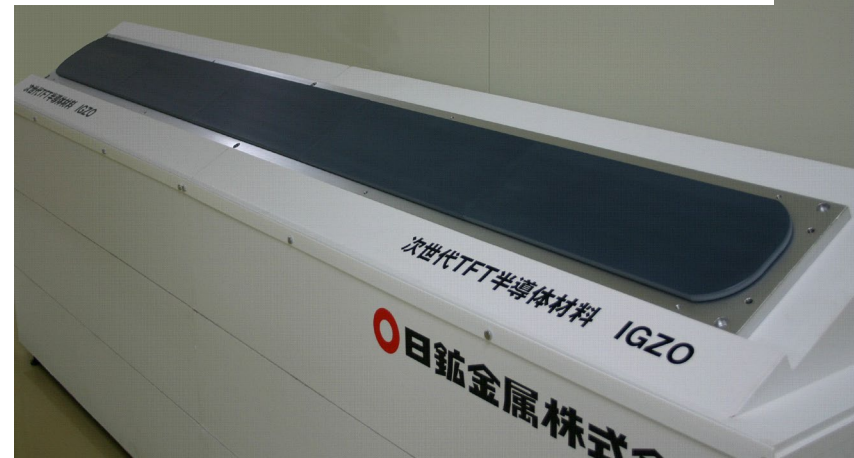
For G8 glass (2.1×2.40 m²)

AKT IGZO sputter

G8.5 rotatory target
AC sputtering (20 – 70 kHz)
Rocking magnet
a-IGZO, a-IZO/a-IGZO, a-ZnON

a-IGZO
Mobility distrib.   8.5–10.0 cm^2/Vs
I_{on} 1.6×10^{-4} A
I_{off} 1.5×10^{-12} A
S ~ 0.8 V/dec
Thickness distrib. <10% for G8
Growth rate 1.8 nm/s

JX Nippon
mining & metals Corp

Figure 1: Rotary target array consisting of 12 Gen8.5 Al5N targets installed at PiVot^{TM} sputter system.

CONTENTS

Operation of field-effect transistor (FET)

Two representative functions of transistor
1. Amplification   Use linear region ($I_{DS} \propto V_{GS}$)
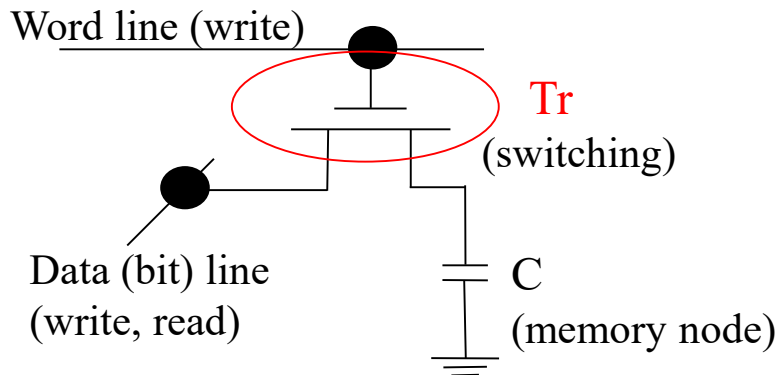2. Switching   Use large on/off current ratio

On current

Off state   On state

Leak current:
power consumption

1C-1Tr memory

Word line (write)

Tr
(switching)

Data (bit) line
(write, read)

C
(memory node)

At $V_{GS} = 0V$
    On state: Normally-on
                Depletion-type
    Off state: Normally-off
                Enhancement-type

TFT structure and operation

Bottom gate, top contact

V_{DS} I_{DS}

Source **Drain**

Semi. (~30 nm)

Insulator (~150 nm)

Gate

n^+ Si

V_{GS}

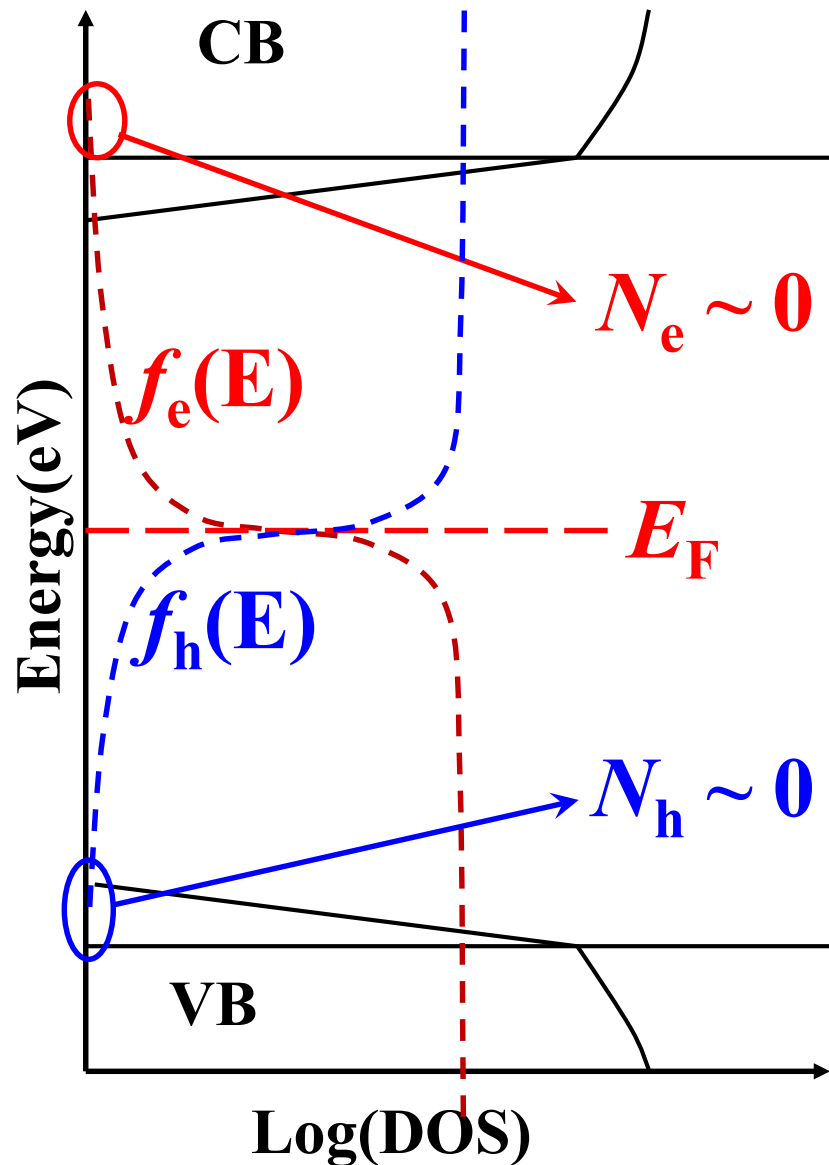$+ +$

$$Q_{ind} \approx C_g (V_{GS} - V_{th})$$

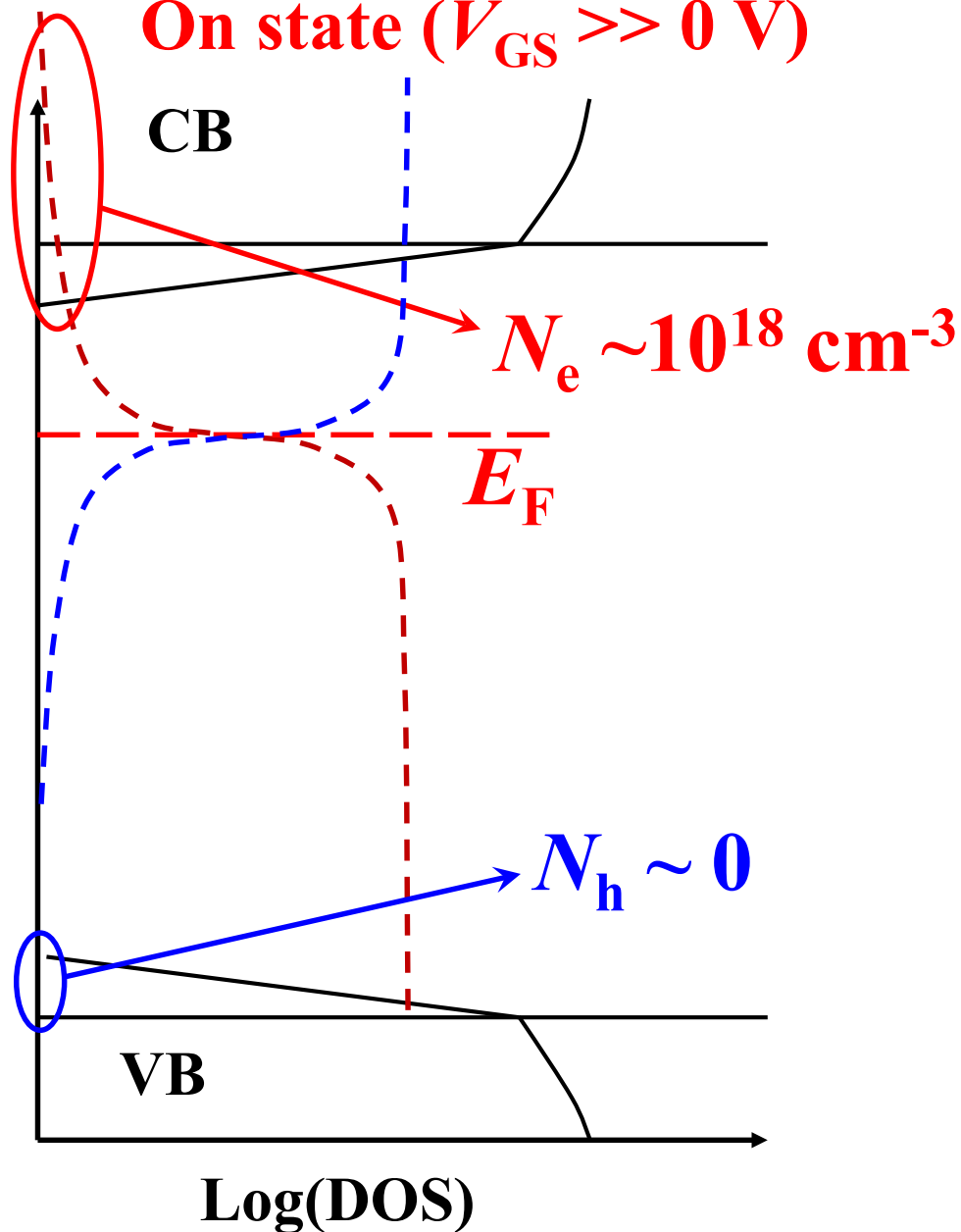$$I_{DS} = \frac{W}{L} \mu_{drift} C_g (V_{GS} - V_{th}) V_{DS}$$

Ideal case

N-channel operation of TFT
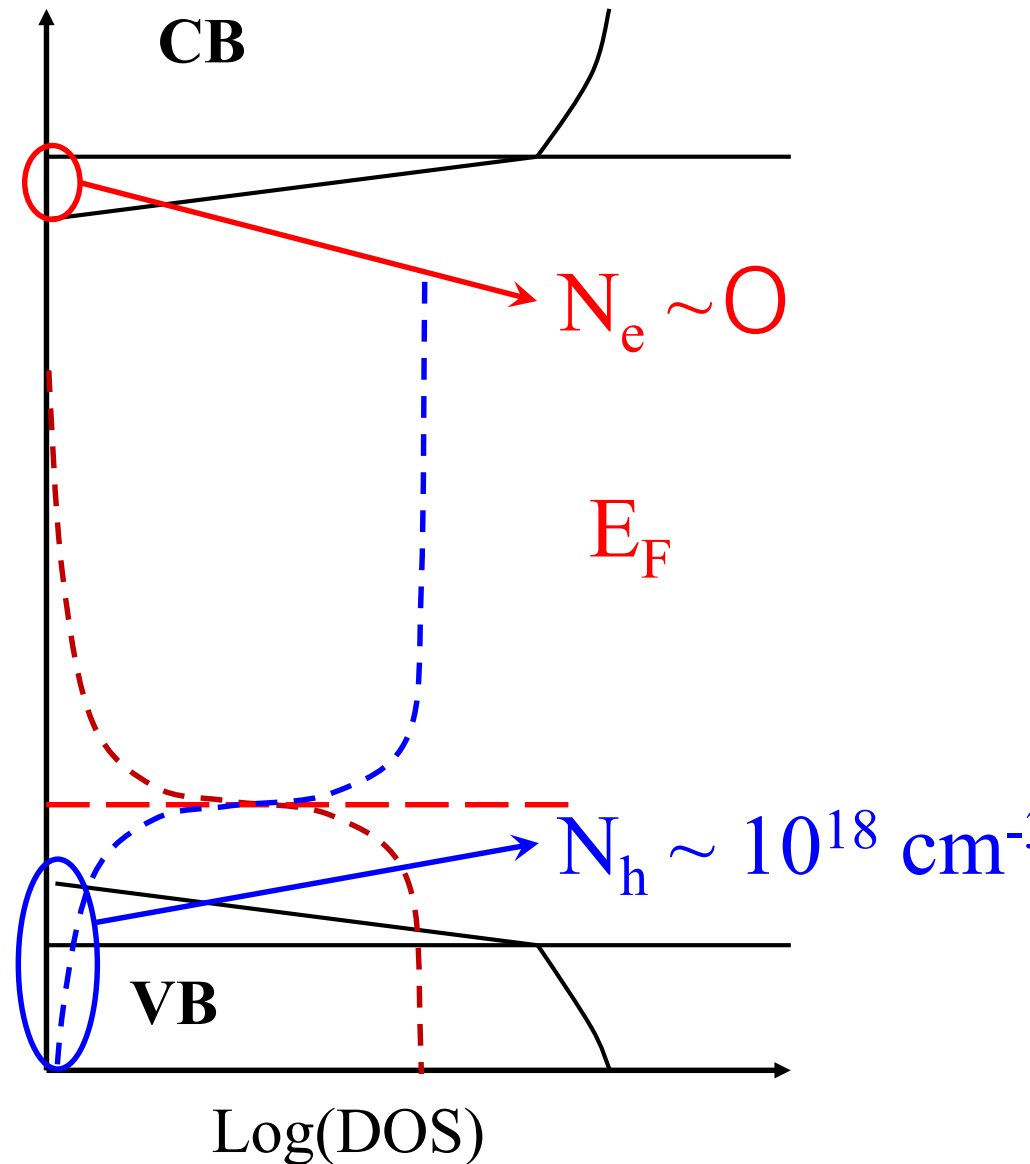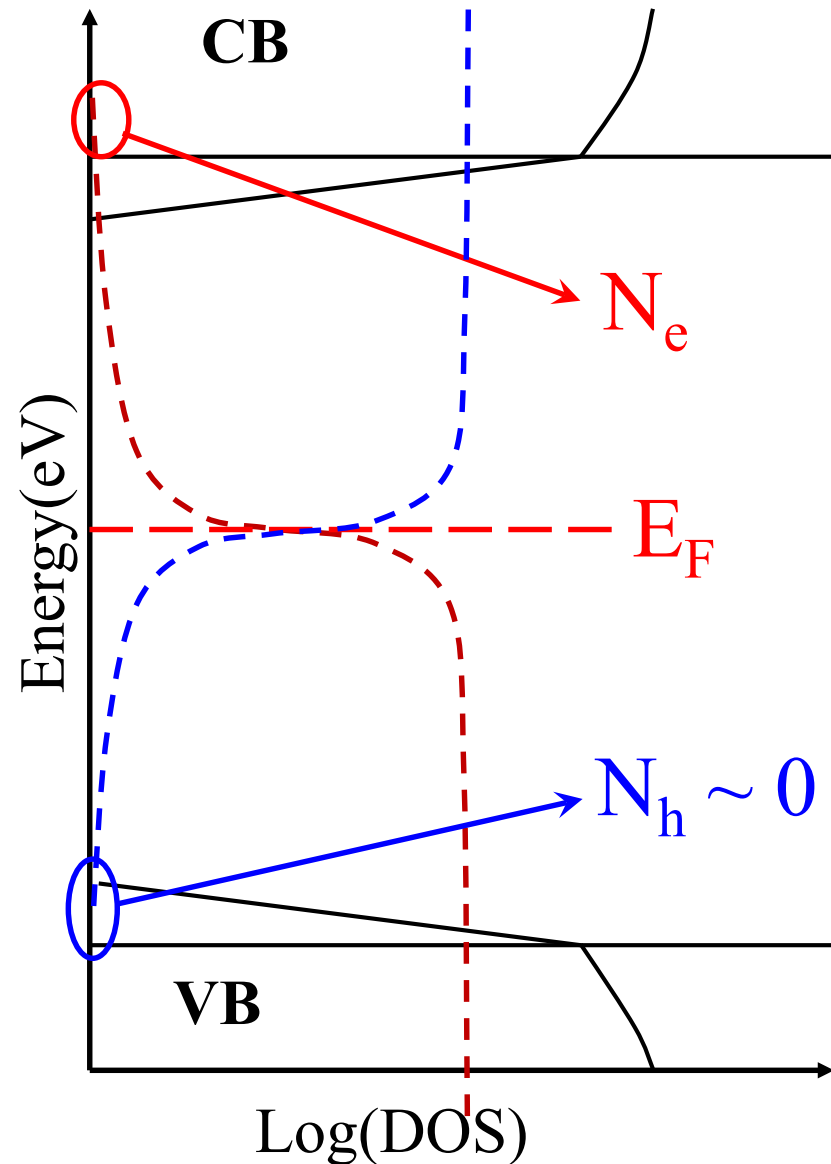
Off state ($V_{GS} \sim 0$ V)

On state ($V_{GS} \gg 0$ V)

CB

CB

$N_e \sim 0$

$N_e \sim 10^{18}$ cm^{-3}
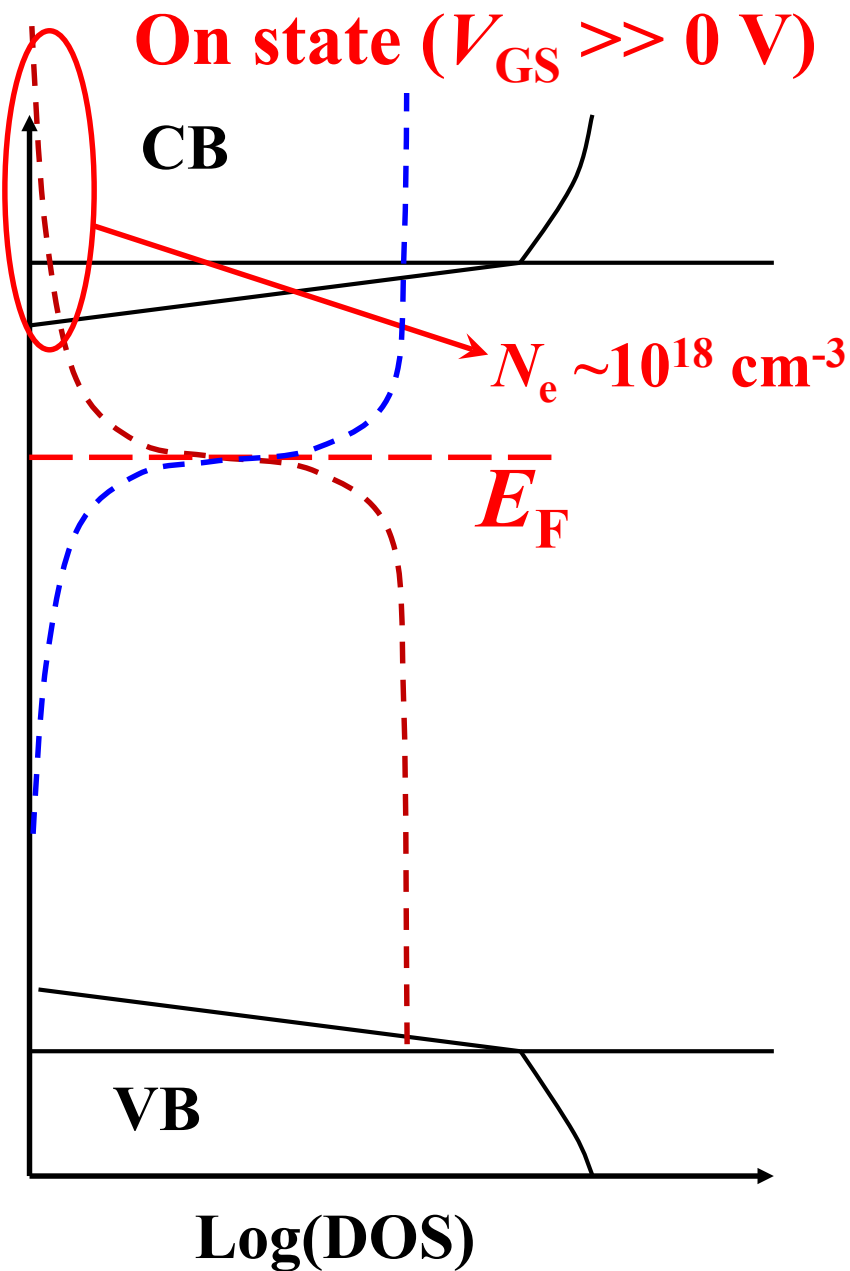
$f_e(E)$

E_F

E_F

$f_h(E)$

$N_h \sim 0$

$N_h \sim 0$

Energy(eV)

VB

VB

Log(DOS)

Log(DOS)

P-channel operation of TFT

Off state (V_GS ~ 0 V)

$$V_{GS} \sim 0\ V$$

CB

N_e

E_F

$N_h \sim 0$

VB

Log(DOS)

On state (V_GS << 0 V)

$$V_{GS} \ll 0\ V$$

CB

$N_e \sim O$

E_F

$N_h \sim 10^{18}\ cm^{-}$

VB

Energy(eV)

Log(DOS)

Fermi level pinning by subgap traps

On state ($V_{GS} \gg 0$ V)

CB

$N_e \sim 10^{18}$ cm^{-3}

E_F

VB

Log(DOS)

On state ($V_{GS} \gg 0$ V)

CB

$N_e = Q_{ind} - N_{trap}$
$< 10^{18}$ cm^{-3}

E_F

N_{trap}
$\sim 10^{18}$ cm^{-3}

VB

Log(DOS)
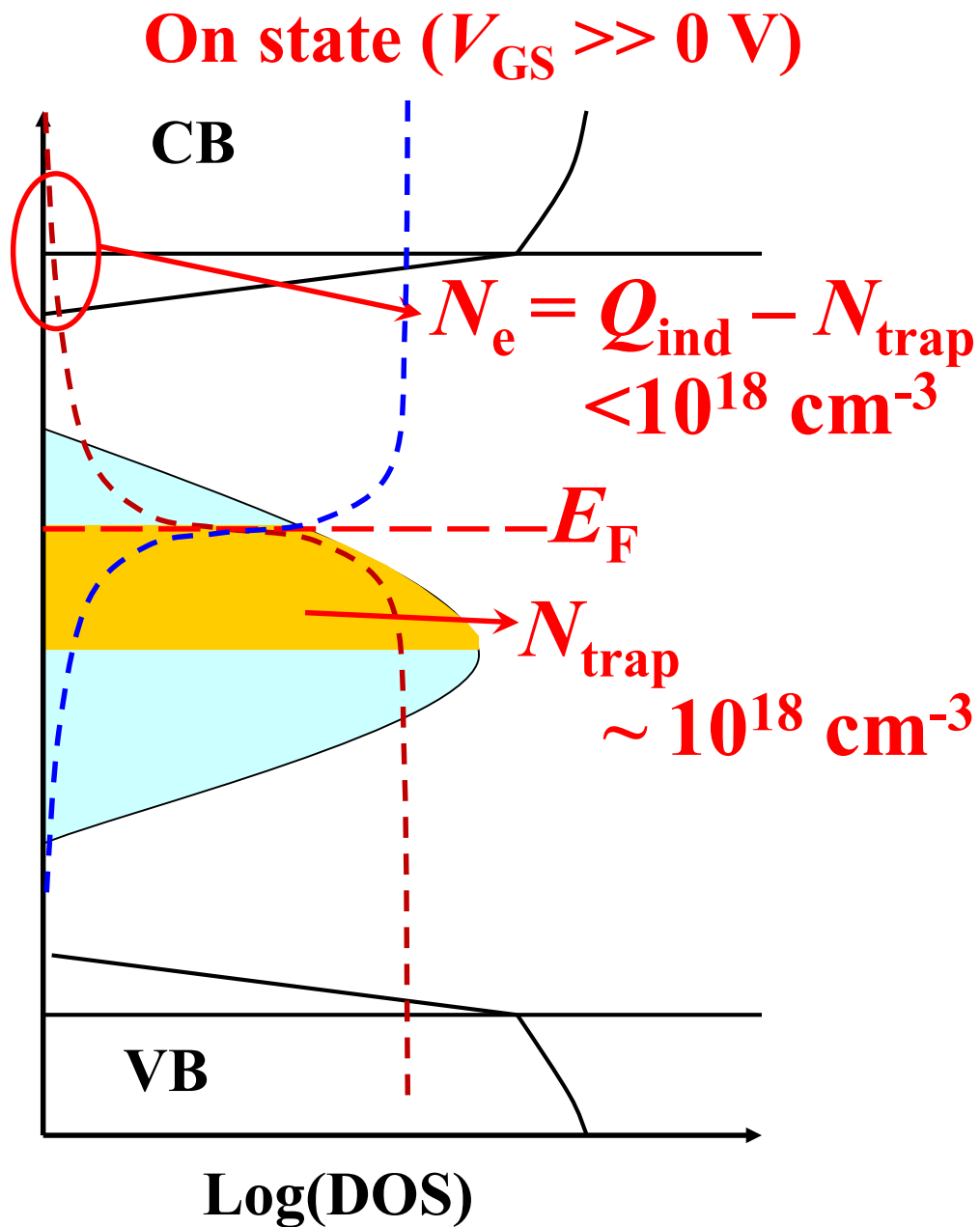
Effect of subgap states (trap states in E_g)

Conduction band

Mobility edge

Tail states

$E_F(V_{GS})$

$E_F(0\ V)$

Subgap states: $D_{sg}(E)$

Tail states

Mobility edge

Valence band

Log(DOS)

Energy(eV)
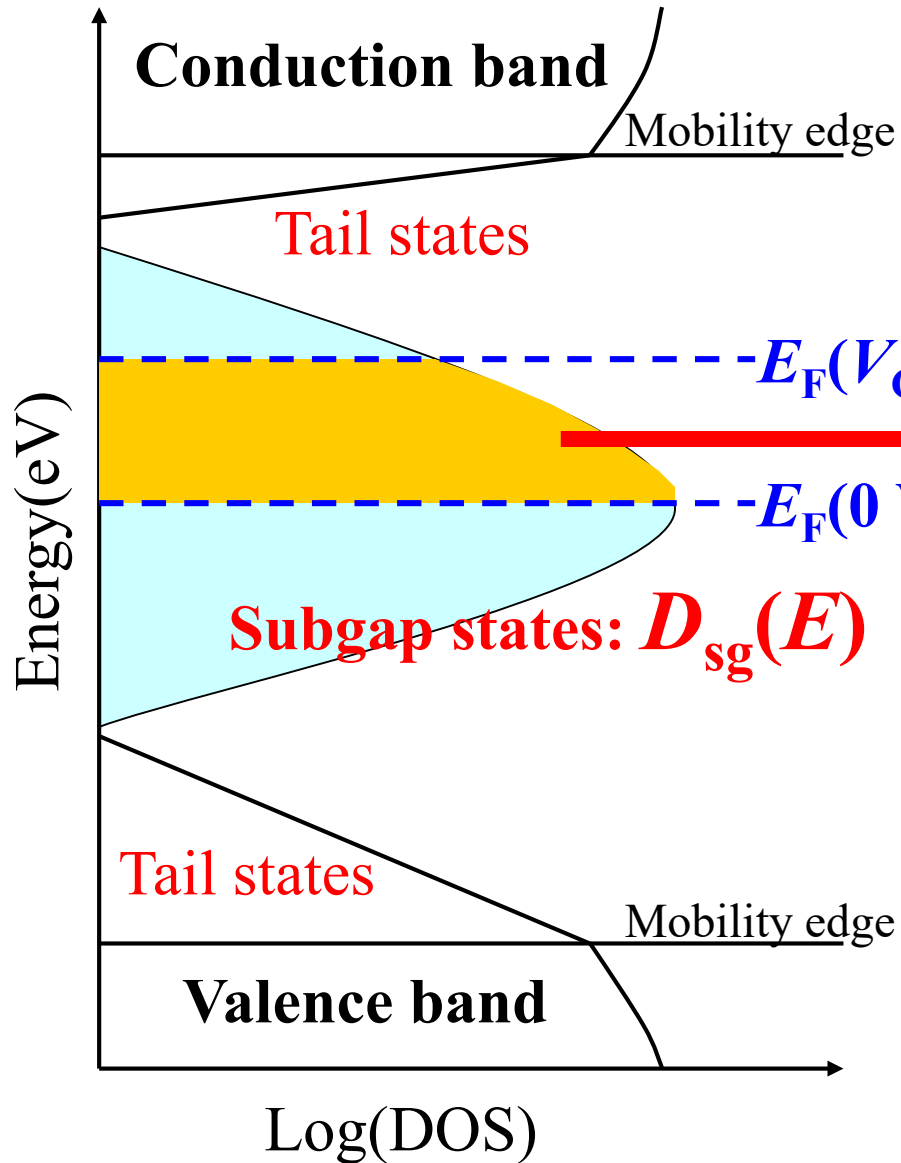
$$I_{DS} = \frac{W}{L}\mu_{drift}C_g\left[(V_{GS}-V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$Q_{ind} \approx C_g V_{GS}$$

$$Q_{sg} = \int_{E_F(0)}^{E_F(V_{GS})} D_{sg}(E)dE$$

$$I_{DS} = \frac{W}{L}\mu_{FE}C_g\left[(V_{GS}-V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$$
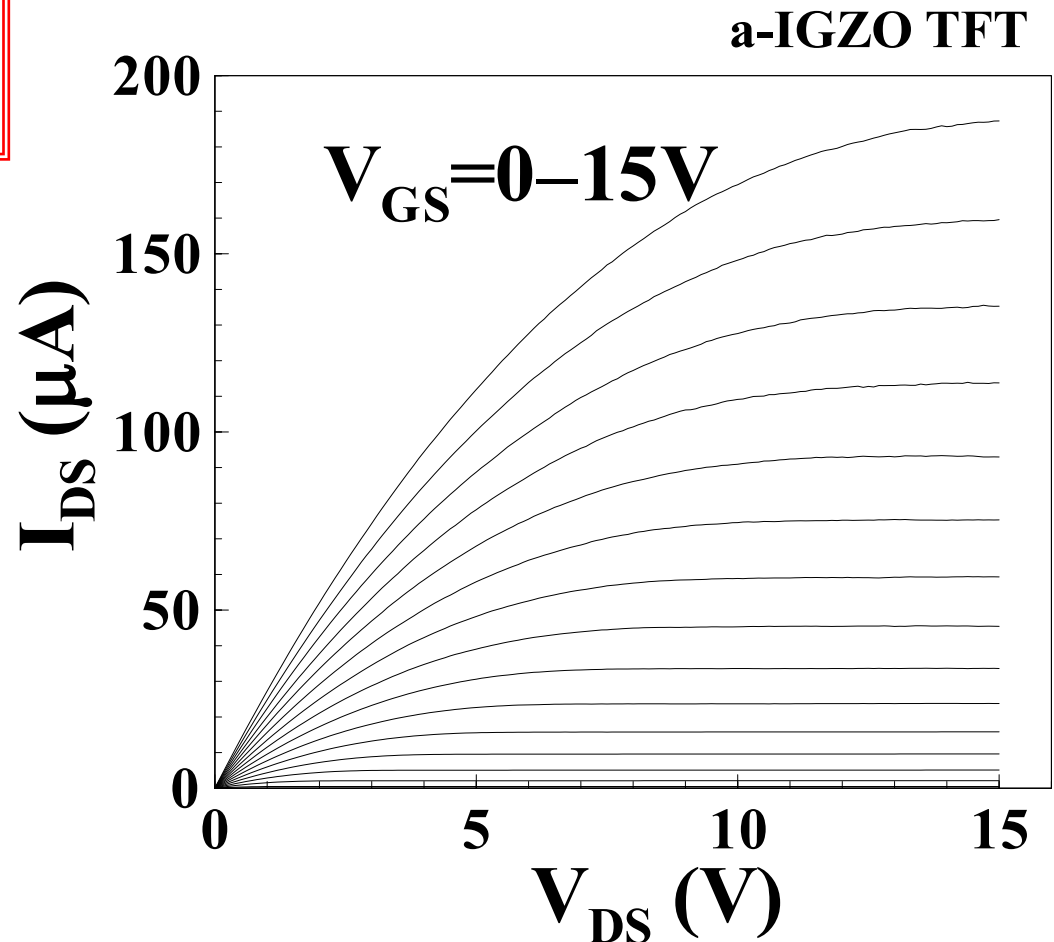
$$\mu_{FE} = \mu_{drift}\frac{Q_{ind}-Q_{sg}}{Q_{ind}}$$

$Q_{ind} \sim 10^{18}$ cm^{-3} (100ppm)
Q_{sg} must be $\ll Q_{ind}$

How to get high-performance TFT?

$$I_{DS} = \frac{W}{L}\mu_{FE}C_g\left[(V_{GS}-V_{th})V_{DS}-\frac{V_{DS}^2}{2}\right]$$

$$\mu_{FE} = \mu_{drift}\frac{Q_{ind}-Q_{sg}}{Q_{ind}}$$

a-IGZO TFT

To obtain high I_{DS}
- Large *W/L* ratio
- Large C_g
- High *V*
- **Large μ_{drift}**
  (Drift mobility)

$$\sigma = en\mu_{drift}$$

- **Low trap density**

V_{GS}=0–15V

Device simulation: TFT and drift mobilities

From Hall ($N_{e,Hall}$) & TFT ($\mu_{FE,sat}$) characteristics   a-In-Ga-Zn-O TFT

$N_{e,Hall}$ (cm^{-3})	$\mu_{FE,sat}$ (cm^2/Vs)	V_{th} (V)
$\sim 1 \times 10^{15}$	**7.84**	4.9

From device simulation (drift mobility)

n_0 (cm^{-3})	μ_{drift} (cm^2/Vs)
1×10^{15}	**8.57**

12% of induced charges are trapped
⇔ >90% for a-Si:H TFT

$V_{GS} = 0 - 15$ V

$V_{DS} = 2 - 10$ V
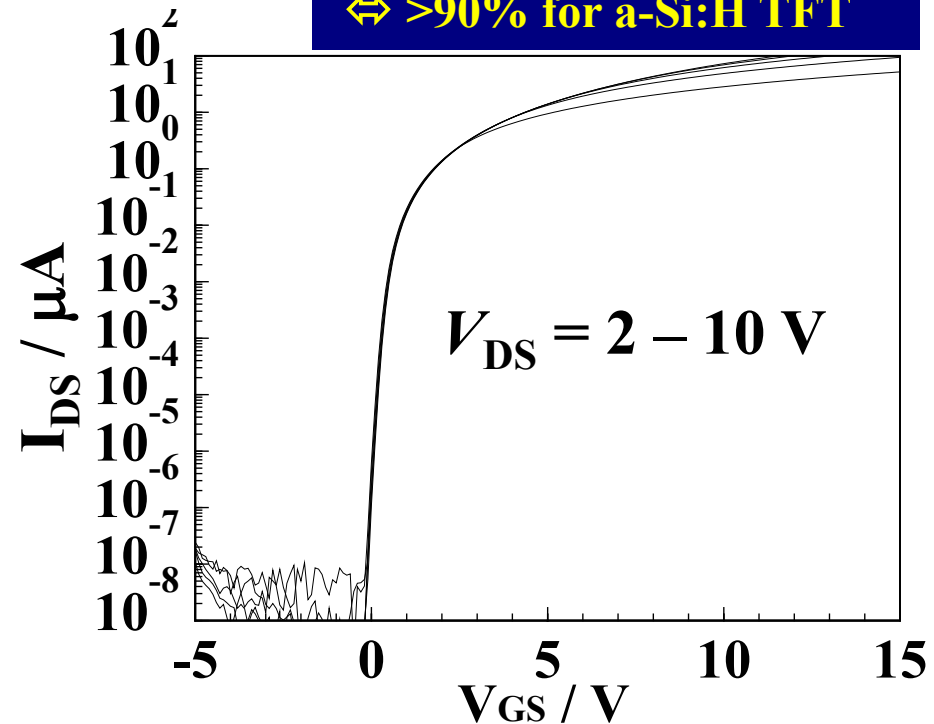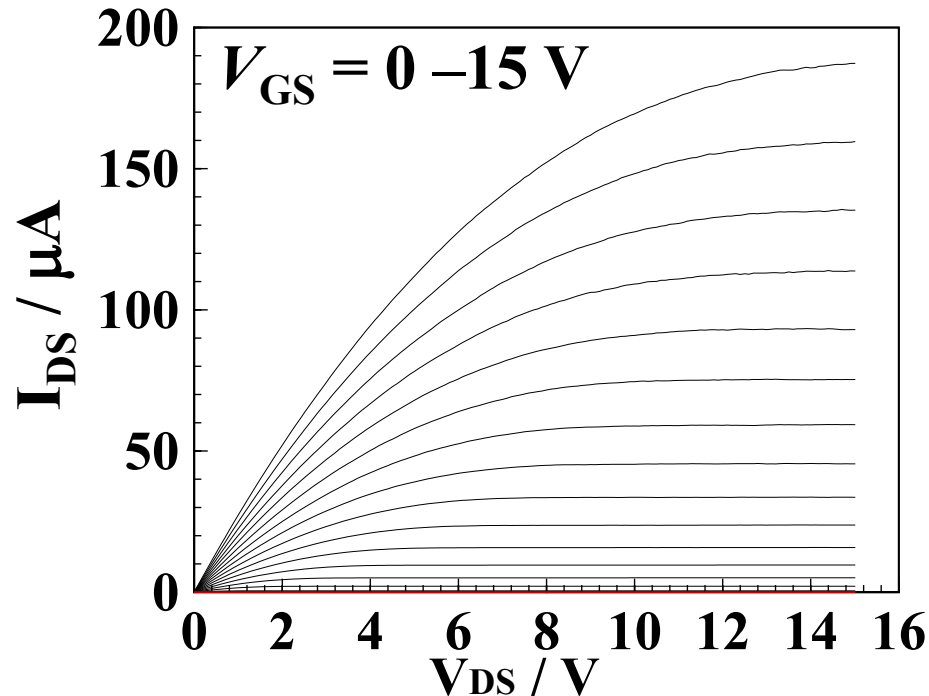
FET analysis: Saturation region

Gradual channel approximation

$$I_{DS} = \frac{W}{L} \mu C_g \left[\left(V_{GS} - V_{th} \right) V_{DS} - \frac{V_{DS}^2}{2} \right]$$
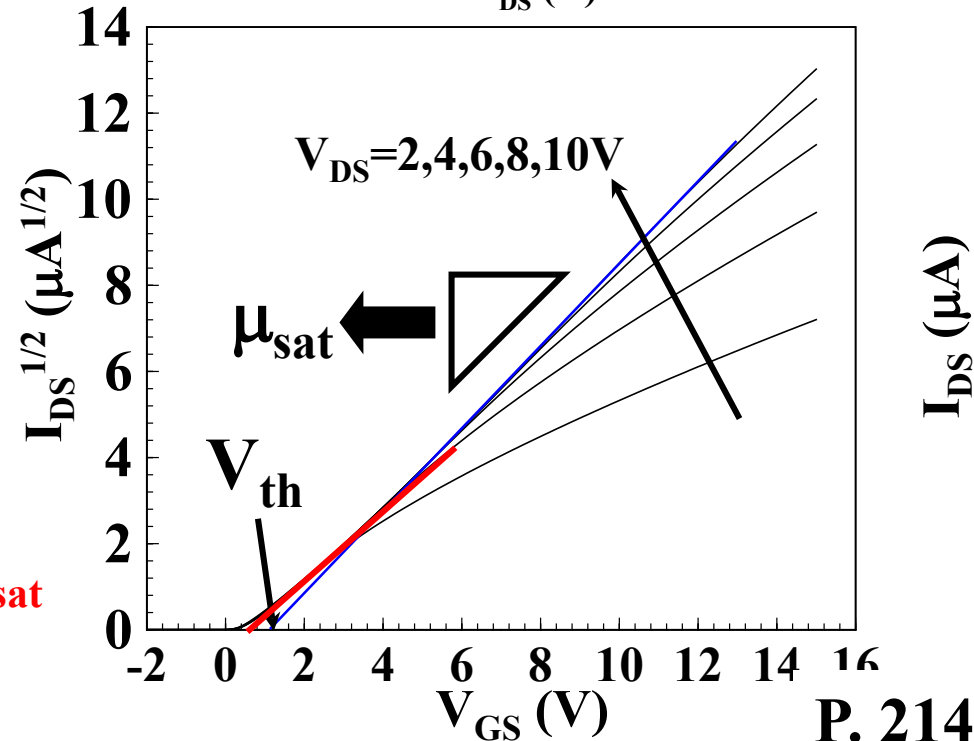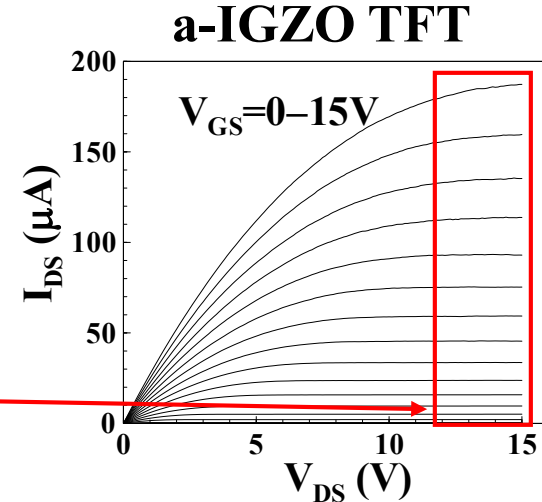
$$V_{DS} > V_p = V_{GS} - V_{th}$$

a-IGZO TFT

$$I_{DS} = \frac{W}{2L} \mu C_g \left(V_{GS} - V_{th} \right)^2$$

$$I_{DS}^{1/2} = \sqrt{\frac{W}{2L} \mu C_g} \left(V_{GS} - V_{th} \right)$$

Plot $I_{DS}^{1/2}$ vs. V_{GS}
  V_{GS} **cross-section:** V_{th}
  Slope: Saturation mobility, μ_{sat}

P. 214

FET analysis: Linear region

$$I_{DS} = \frac{W}{L}\mu C_g\left[\left(V_{GS} - V_{th}\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

I_{DS} (μA) vs. V_{DS} (V), $V_{GS} = 0-15V$

V$_{DS}$ << V$_p$(V$_{GS}$) (e.g., << 0.1 V)
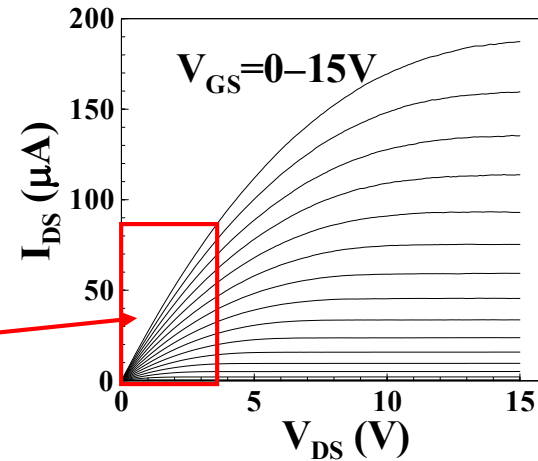
$$I_{DS} = \frac{W}{L}\mu C_g V_{DS}\left(V_{GS} - V_{th}\right)$$

I_{DS} **is proportional to V_{DS}:**
  Plot I_{DS} vs. V_{GS}
    V_{GS} cross-section: V_{th}
      Slope: Linear-regime mobility

Effective mobility: μ_{eff}

$$\mu_{eff} = g_{DS}\frac{L}{WC_g\left(V_{GS} - V_{th}\right)}$$

$$g_{DS} = \frac{dI_{DS}}{dV_{DS}}$$ **Drain conductance**

Field-effect mobility: μ_{FE}

$$\mu_{FE} = g_m\frac{L}{WC_g V_{DS}}$$

$$g_m = \frac{dI_{DS}}{dV_{GS}}$$ **Transconductance**
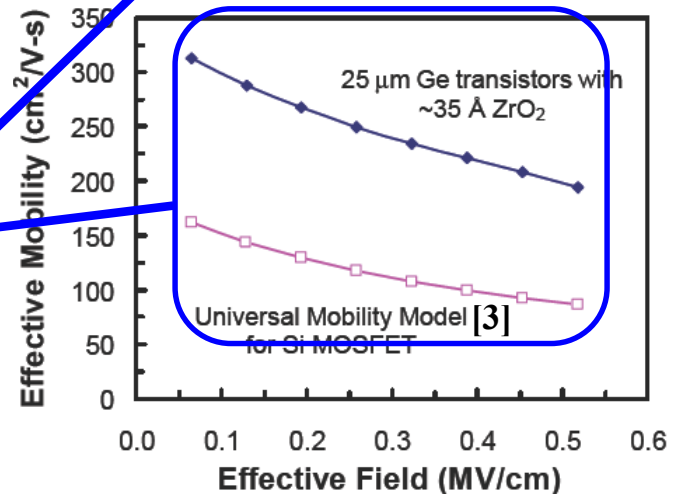
Mobility vs. V_{GS}

a-IGZO TFT / SiO$_2$/c-Si

V_{DS}=2,4,6,8,10V
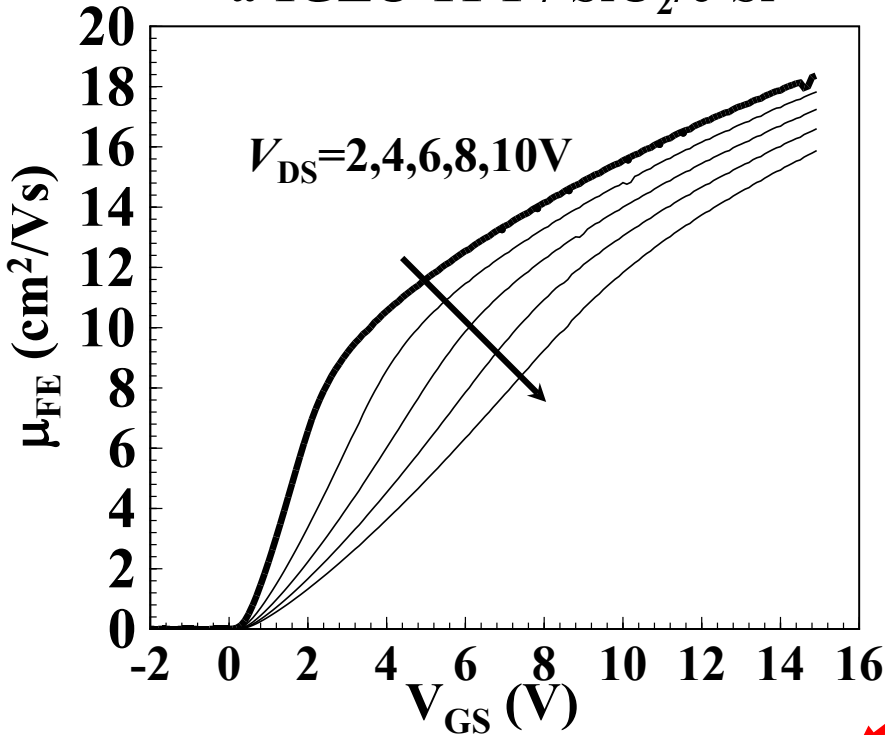
a-IGZO TFT / SiO$_2$/MoW/glass [1]

etch-stopper inverted-staggered

MOSFET [2]

Low V_{GS} : Deteriorated by traps

High V_{GS}: Deteriorated by interface scattering

[1] M.Kim et al., APL **90**, 212114 (2007)

[2] C.O. Chui, H. Kim, D. Chi, B.B. Triplett, P.C. McIntyre, K.C. Saraswat, IEDM (2002) p.437

[3] K. Chen, H. C. Wann, P. K. Ko, and C. Hu, IEEE Electr. Dev. Lett., **17**, 202 (1996)

CONTENTS

Memory: Current shutter

DRAM

Transistor
(switch)

V_{sw}

V_C

C, Q_C
(Memory node)

$$V_C = Q_c / C$$

"1"

Leak

I_{leak}

"0"

Flash memory

V_w

Insulator

Memory node C, Q_C

read

"1"

Transistor: DRAM
Insulator: Flash

"0"

Retention time ~ Q_C / I_{leak}

An issue of Si electronics

Band gap

c-Si: 1.12 eV ($\sigma > 10^{-6}$ Scm^{-1})

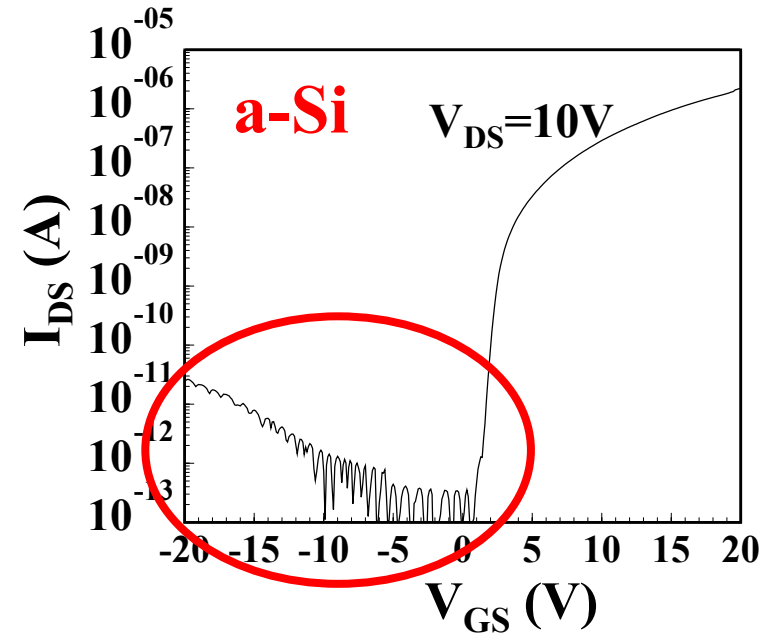a-Si: 1.75 eV *($\sigma > 10^{-15}$ Scm^{-1} ?)*

I_{leak}

MOSFET : $< 10^{-9}$ A

DRAM refresh time: several ms

Poly-Si TFT: $< 10^{-11}$ A

a-Si TFT : $< 10^{-13}$ A

Retention time: tens seconds at most

An issue of Si electronics

Band gap

  c-Si: 1.12 eV ($\sigma > 10^{-6}$ Scm^{-1})

  a-Si: 1.75 eV *($\sigma > 10^{-15}$ Scm^{-1} ?)*

I_{off}

  MOSFET   : < 10^{-9} A

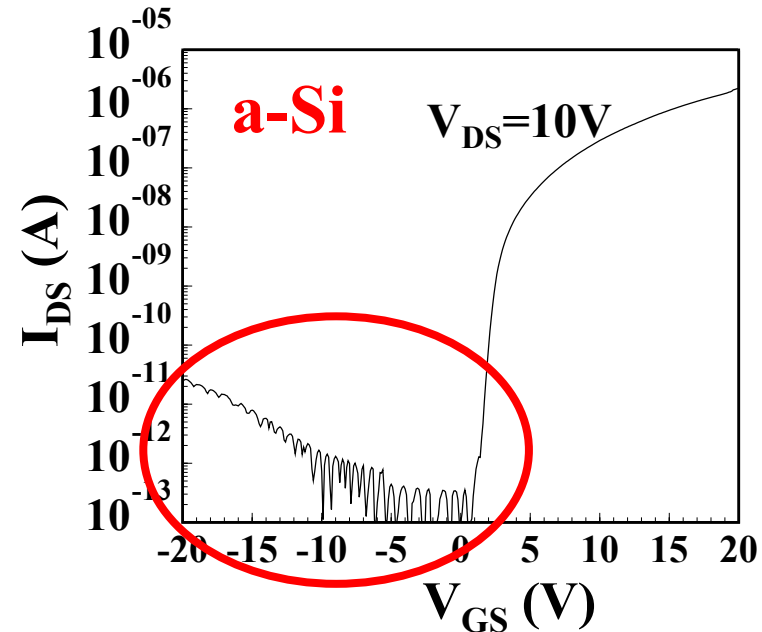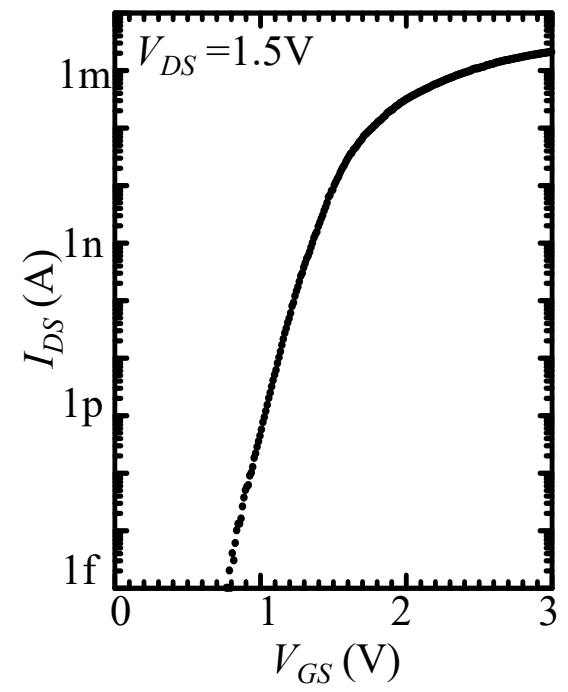 **DRAM refresh time: several ms**

  Poly-Si TFT: < 10^{-11} A

  a-Si TFT   : < 10^{-13} A

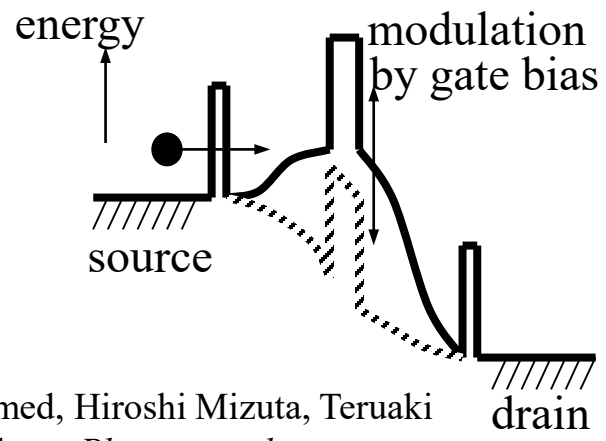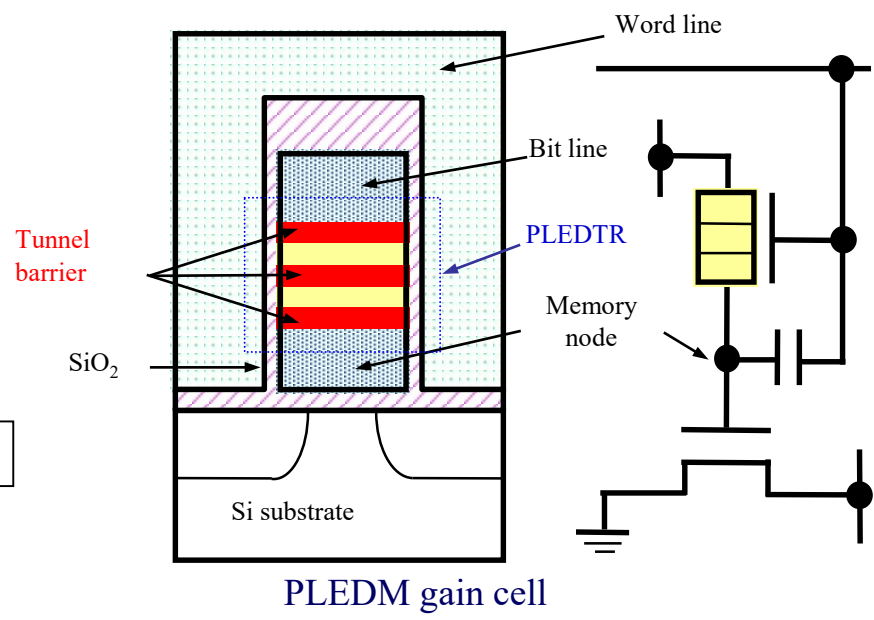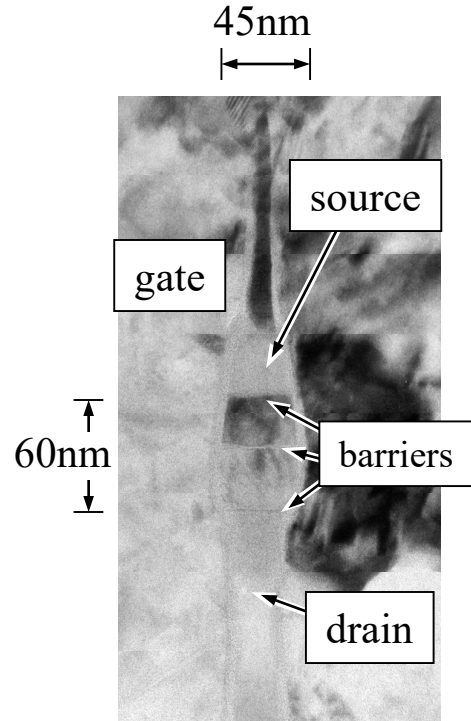 **Retention time: tens seconds at most**

a-IGZO?

  Lower & constant I_{off}, << 10^{-15} A

Non-volatile devices proposed
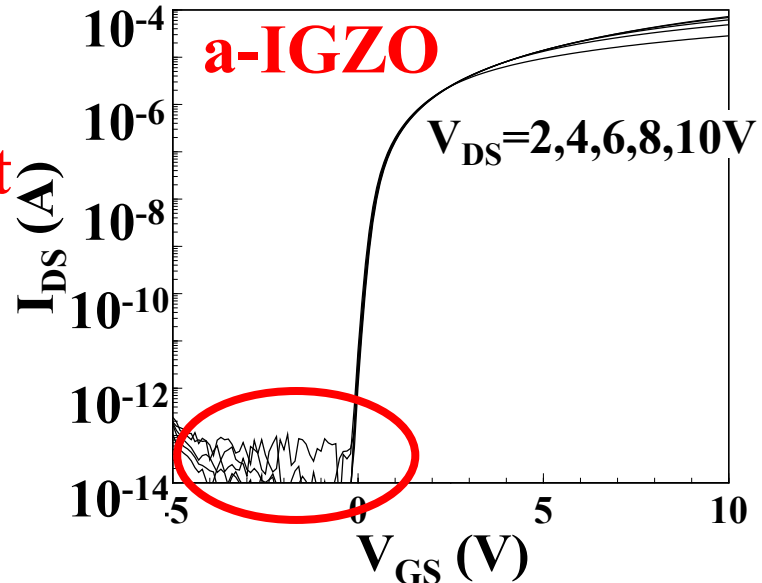
PLEDM® (Phase-state Low Electron-number Drive Memory)

45nm

source

gate

60nm

barriers

drain

Word line

Tunnel barrier

Bit line

PLEDTR

Memory node

SiO$_2$

Si substrate

PLEDM gain cell

energy

modulation by gate bias

source

drain

$V_{DS} = 1.5V$

I_{DS} (A)

1m

1n

1p

1f

0   1   2   3

V_{GS} (V)

Kazuo Nakazato, Kijoo Itoh, Haroon Ahmed, Hiroshi Mizuta, Teruaki Kisu, Masataka Kato and Takeshi Sakata: *Phase-state low electron-number drive random access memory (PLEDM)*; 2000

	requirement	I_{ON}	I_{OFF}
MOSFET	high drivability	**>30 mA**	<1nA
PLEDTR	low leakage	>0.1 mA	**<1fA**

Low-power Display System Driven by Utilizing Technique Using Crystalline IGZO Transistor

Tatsuji Nishijima, Seiichi Yoneda, Takuro Ohmaru, Masami Endo, Hiroki Denbo, Masashi Fujita, Hidetomo Kobayashi, Kazuaki Ohshima, Yutaka Shionoiri, Kiyoshi Kato, Yukio Maehashi, Jun Koyama, and Shunpei Yamazaki
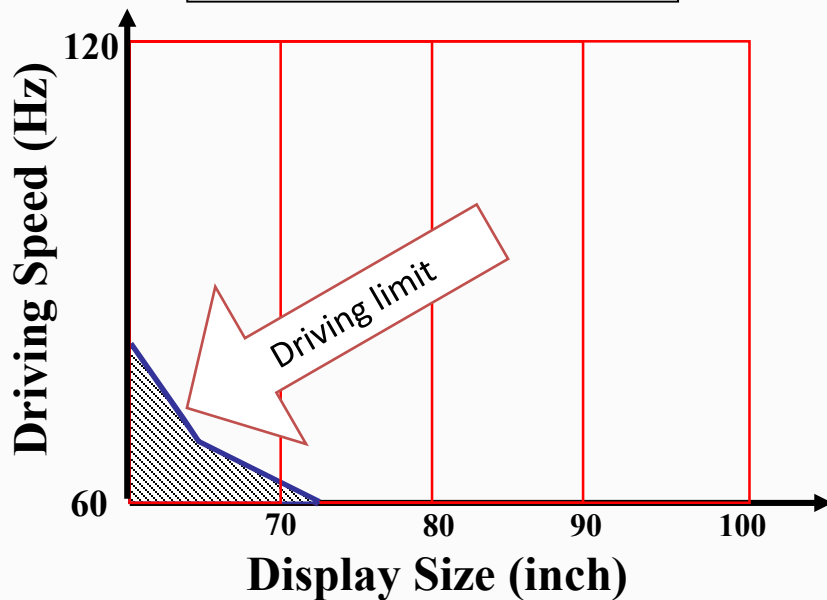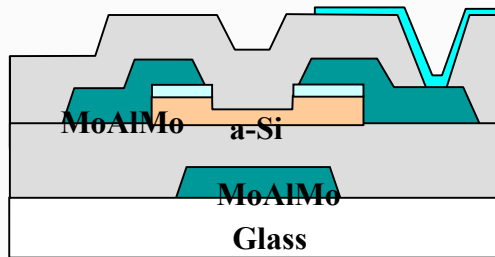
SID2012, 43.1
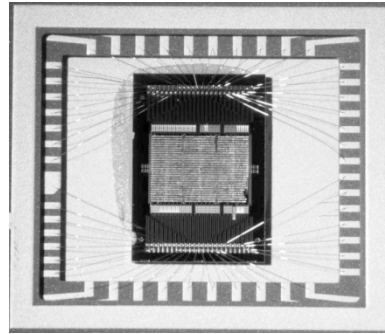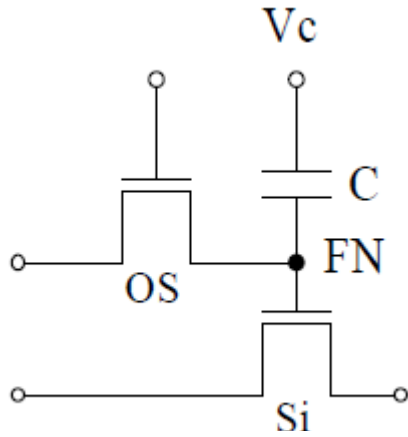
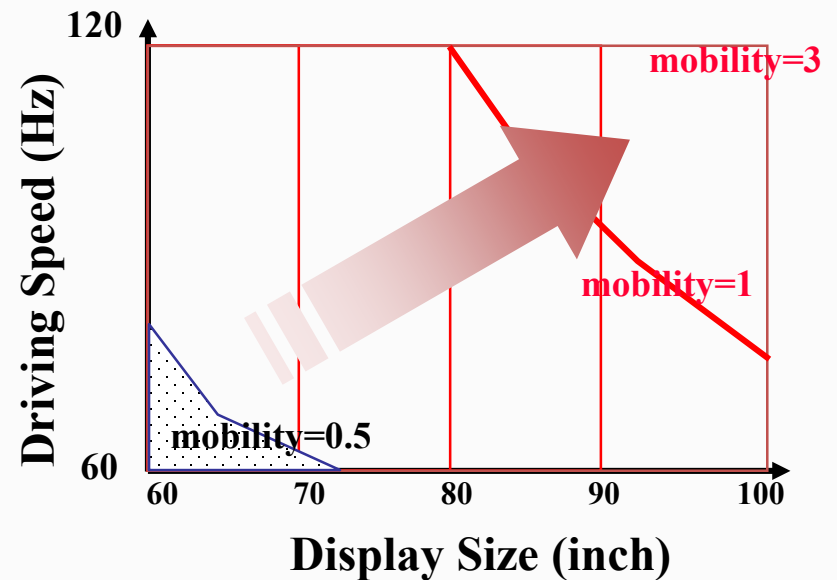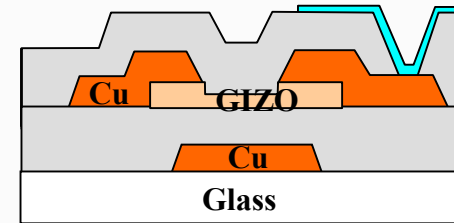**Non-volatile DRAM**
Normally-off CPU
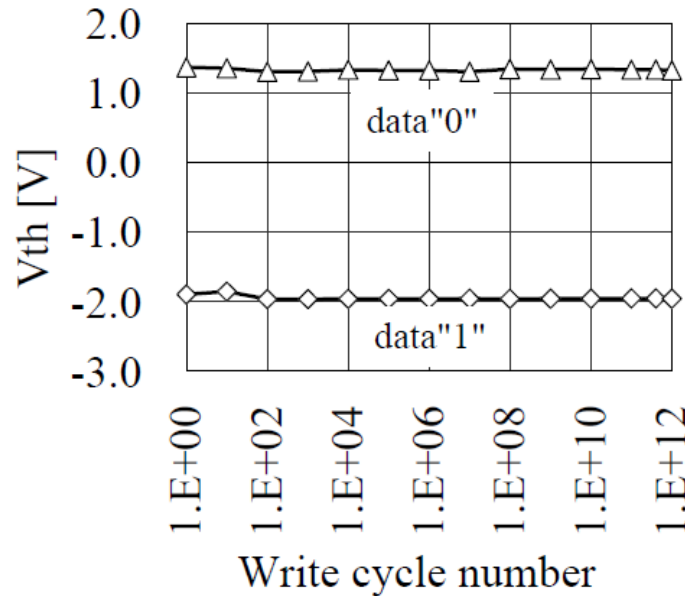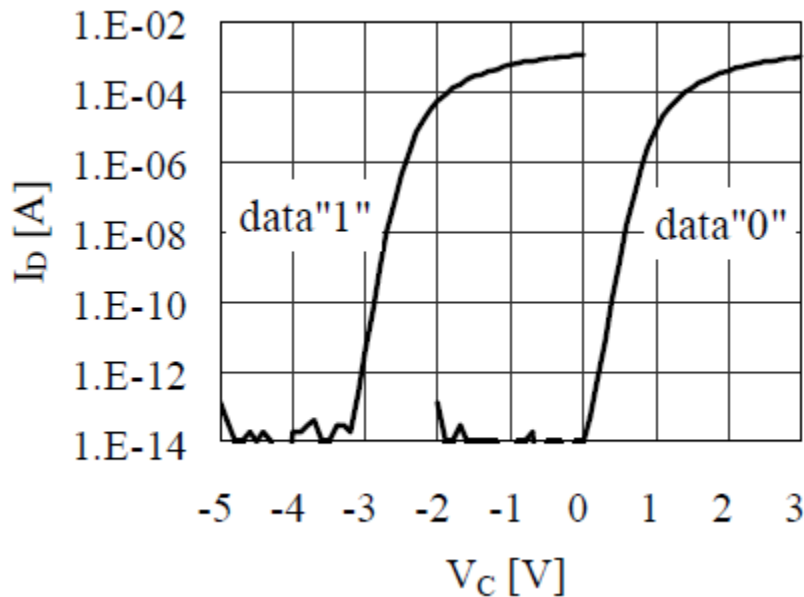
Trend in AM-LCD panels and demanding TFT performance

Source : Jang Yeon Kwon (SAIT), IDW 2007

Conventional a-Si TFT

High mobility TFT

Issues for OLED

2Tr driving circuit

Metal cap

Getter

Metal cathode   Inert gas

Organic Layer

Anode

Planarization layer

Driving TR

Glass Substrate

Pixel Driving Circuit

current source

selection

Sw Tr

data line

V_{DATA}

G

D

Drv Tr

S

V_G

V_{EL}

Light emission

I

cathode
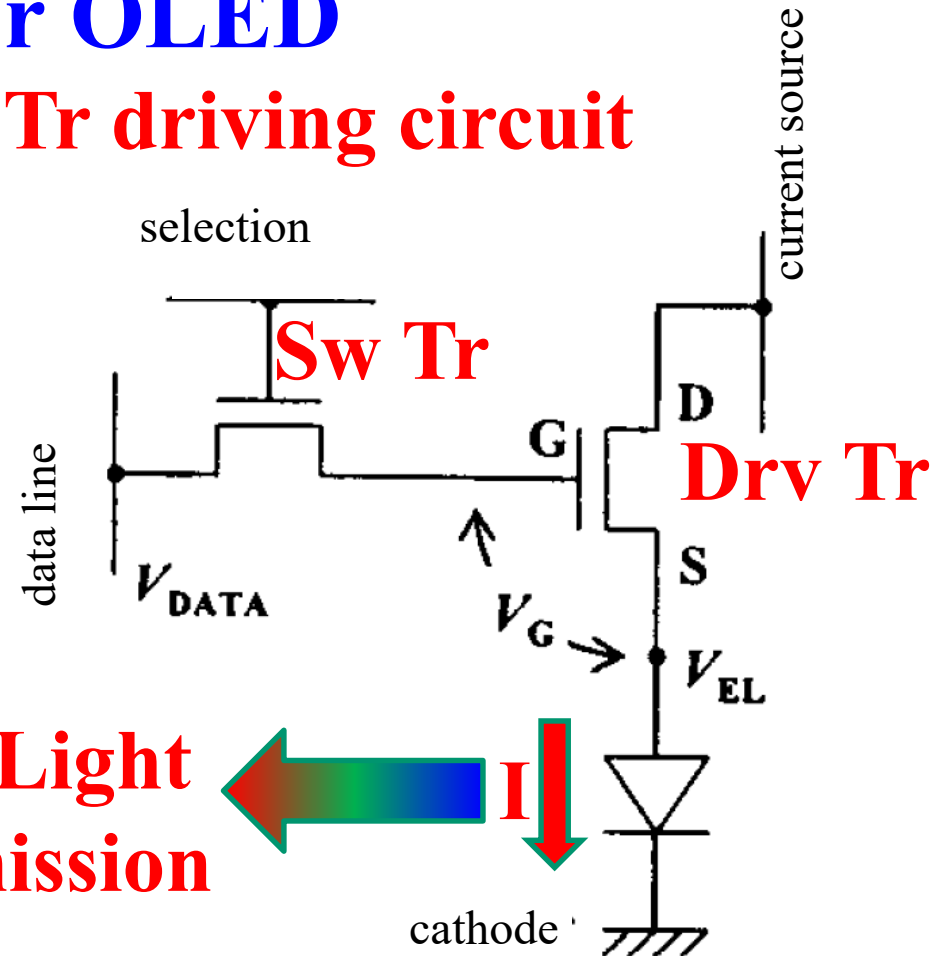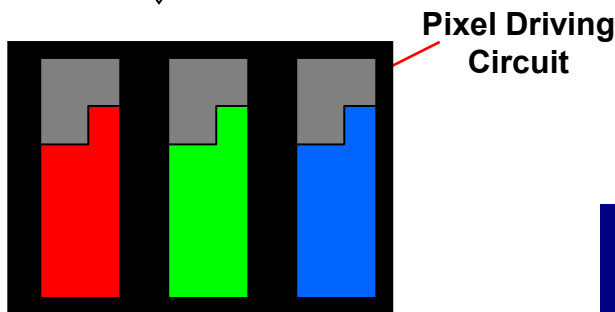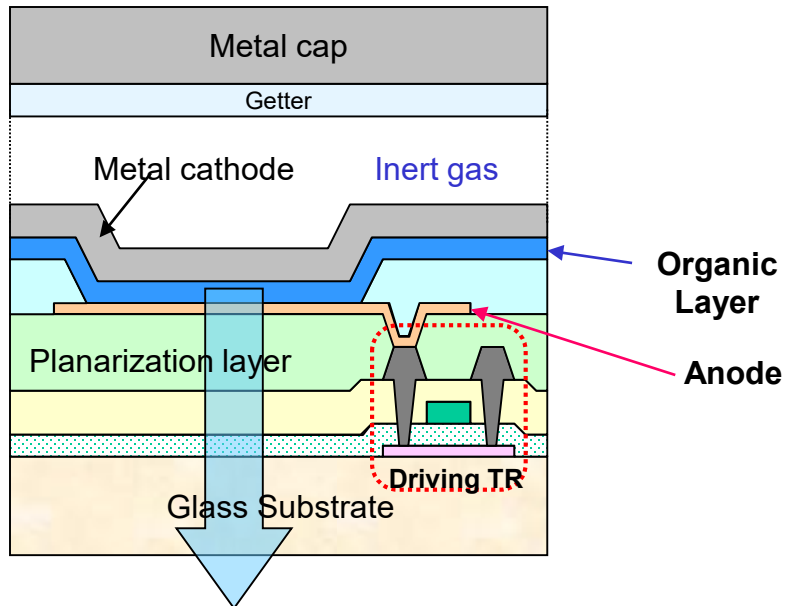
Switching Tr: Charge to a driving Tr
Driving Tr: Current flow for light emission
High current drivability, High mobility
(> 4 cm^2/Vs) are required for the driving Tr

Effect of V_{th} shift on AMOLED

Simplest 2Tr+1C pixel circuit

V_{data} V_{dd} for EL

Gate line

I_{DS}

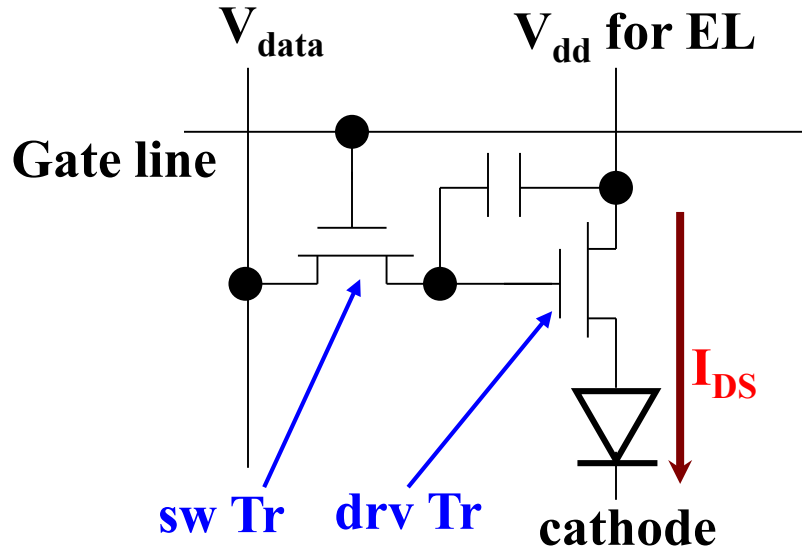sw Tr   drv Tr   **cathode**

Luminance, L
$\propto I_{DS}$
$\propto (V_{data} - V_{th})^2$

V_{data}

Calculation of luminance

Assume:

$\mu = 10$ cm^2/Vs, $C_i = 3\times10^{-8}$ F/cm^2

W = 20 μm, L = 10 μm

$V_{data} = 4$ V, $V_{th} = 1$ V

$$L \propto I_{DS} = \left(\mu W C_i / L\right)\left(V_{data} - V_{th}\right)^2$$

For ± 0.1 V V_{th} variation

$I_{DS} = 2.7$ μA for $V_{th} = 1.0$ V

$I_{DS} = 2.9$ μA for $V_{th} = 1.1$ V

16 % change of luminance

=> 'MURA' problem

Non-uniformity issue in OLED

Light luminance

proportional to $(V - V_{th})^2$

Fluctuation of 0.1 V in V_{th} causes

16 % change in luminance
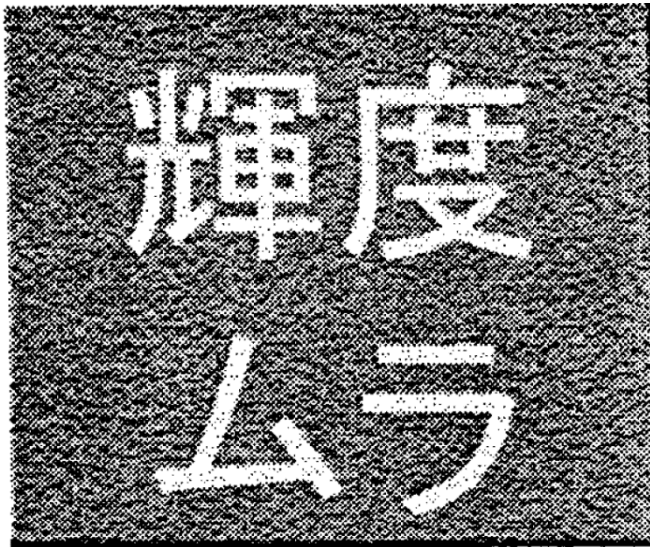
Mura   Image sticking
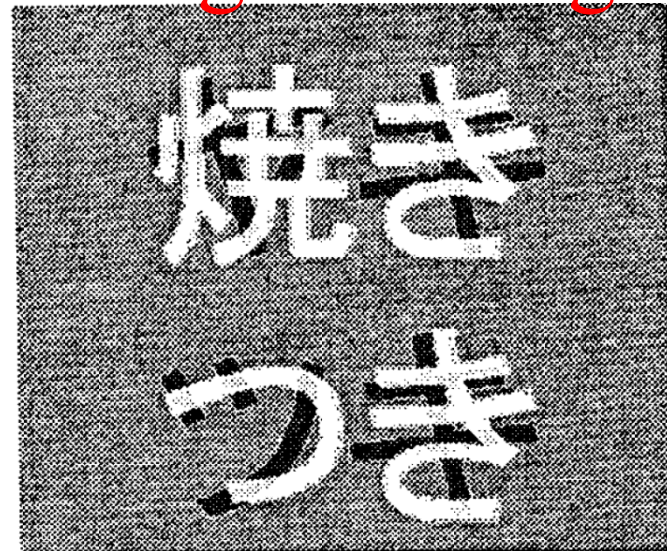
Extra circuits needed for present OLED

Metal cap

Getter

Metal cathode   Inert gas

→ **Organic Layer**

Planarization layer

↗ **Anode**

Driving TR

Glass Substrate

Pixel Driving Circuit
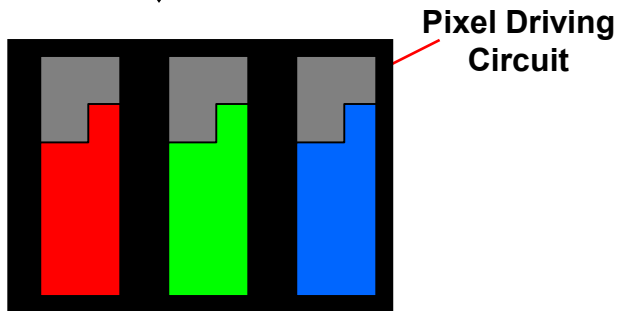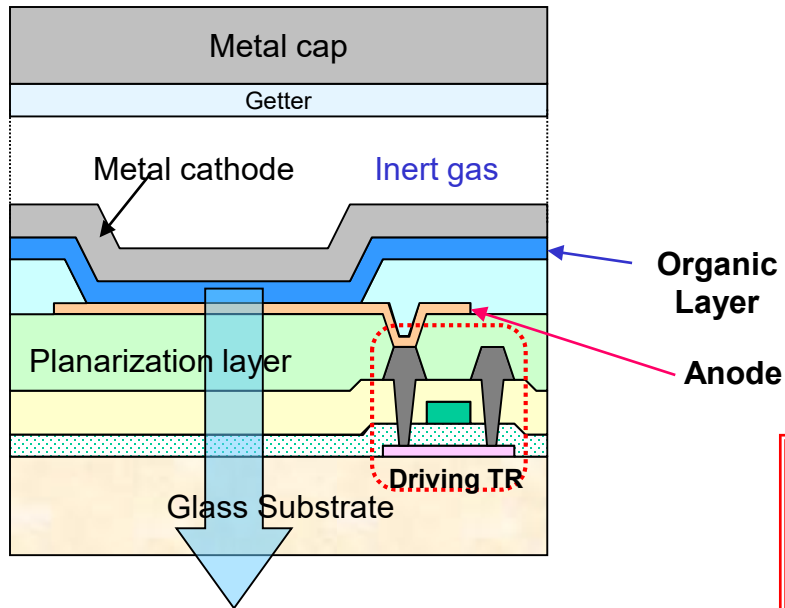
Aperture ratio << 30%

2Tr driving circuit

selection

current source

data line

G   D

V_{DATA} V_G →   S

V_{EL}

cathode
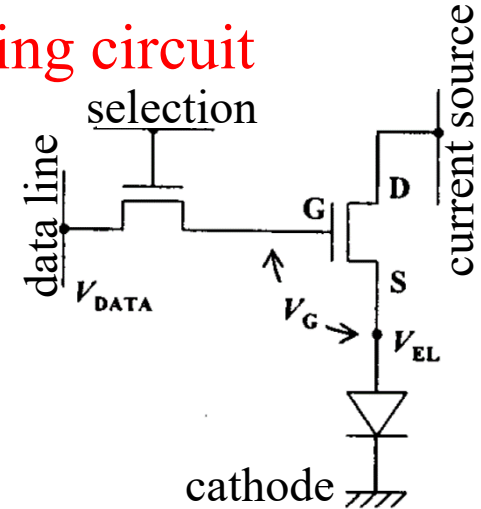
4Tr current compensation circuit

selection   current source

T3

T2

data line C_S

T1

cathode
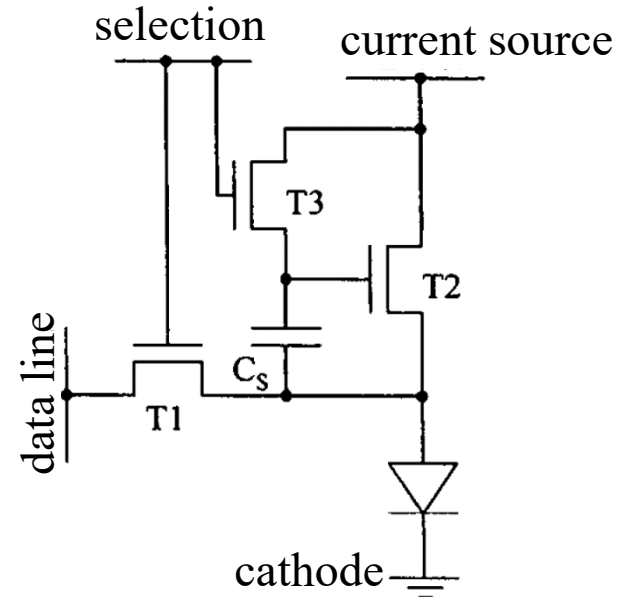
Requirements for TFTs

1. Electronic paper *By courtesy of Dr. Matsueda (AUO)*

Low-T, low-cost fabrication

On-current (mobility) is not critical ($<< 1 \ cm^2/Vs$ is ok)

Off-current is not critical: E-Ink itself has a memory function

Low performance TFT (slow response, $I_{on/off} \sim 10^3$ are OK)

2. Liquid crystal display

Moderately low-T ($\sim 350^oC$), low-cost fabrication

On-current (mobility) is not critical

a-Si:H and organic TFTs ($\mu_{FE} < 1 \ cm^2/Vs$) are OK

Low off-current is favorable: $I_{off} < 10^{-12}$ A is required

3'. Jumbo size / high frame rate ($\geq$480 Hz) / 8K LCD

High on-current ($\mu_{FE} > 3 \ cm^2/Vs$)

3. Organic light-emitting diode display

High on-current ($\mu_{FE} > 4 \ cm^2/Vs$)

Very high stability ($\Delta V_{th} << 1V$)

4. Flexible display

Low-T process ($<< 200^oC$), Flexibility (Brittleness)

CONTENTS

CONTENT for AOS TFT

1. Characteristics of a-IGZO TFT
2. Current AOS displays
3. Materials
4. Growth condition and TFT fabrication
5. Doping
6. Defect structures (subgap defects)
7. Why too large P_{O_2} is bad?:
   Weakly-bonded Oxygen
8. Annealing
9. Hydrogen

CONTENT for AOS TFT

1. **Characteristics of a-IGZO TFT**
2. Current AOS displays
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   Weakly-bonded Oxygen
8. Annealing
9. Hydrogen

Flexible & Transparent a-IGZO TFT

a-InGaZnO$_4$ (a-IGZO)

- ✓ High mobility > 10 cm^2/Vs
- ✓ Large bandgap E_g ~ 3.0 eV
- ✓ Uniformity, Stability
- ✓ Room T process => Flexible

2004

Before binding

8.3 cm^2/Vs

R = 60mm
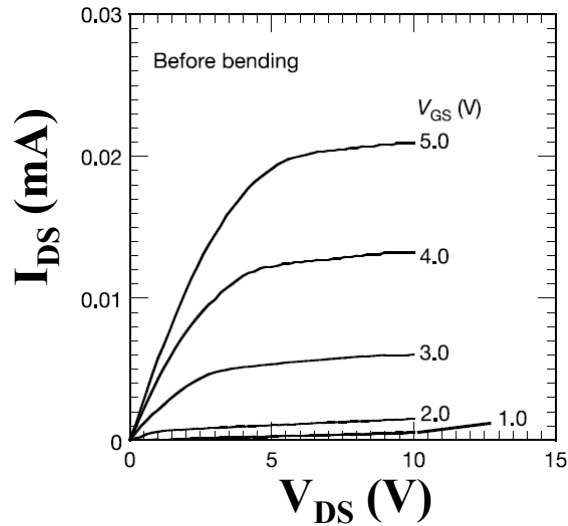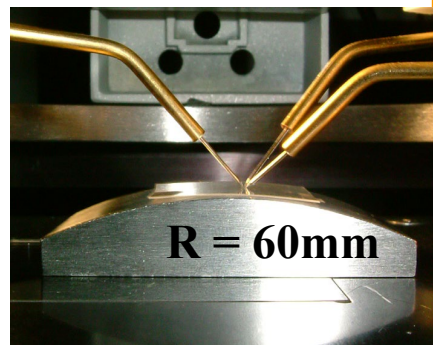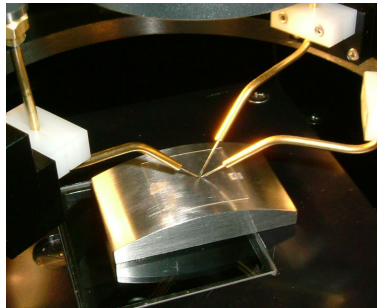
After bending
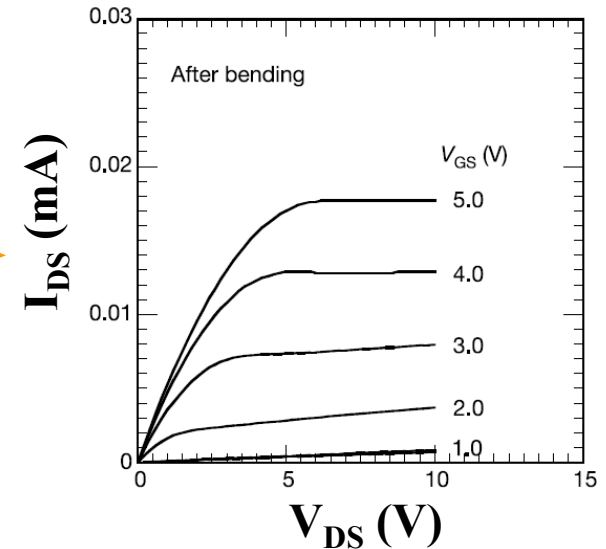
7 cm^2/Vs

a-IGZO TFT vs a-Si:H TFT

a-IGZO: Top-contact, bottom gate 40nm-thick a-IGZO / 150nm-thick SiO_2 / c-Si, W/L = 300/50 (μm)

a-Si:H : Inverted staggered   200nm-thick a-Si:H / 200nm-thick SiN_x, W/L = 28/6 (μm)
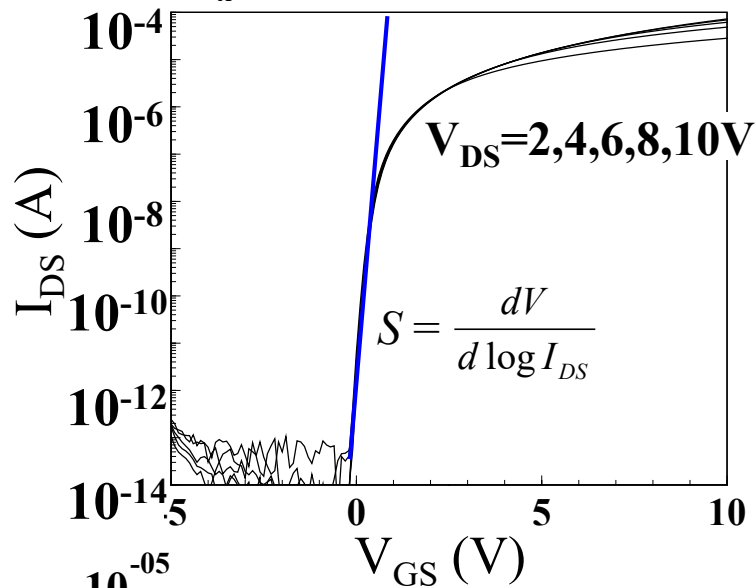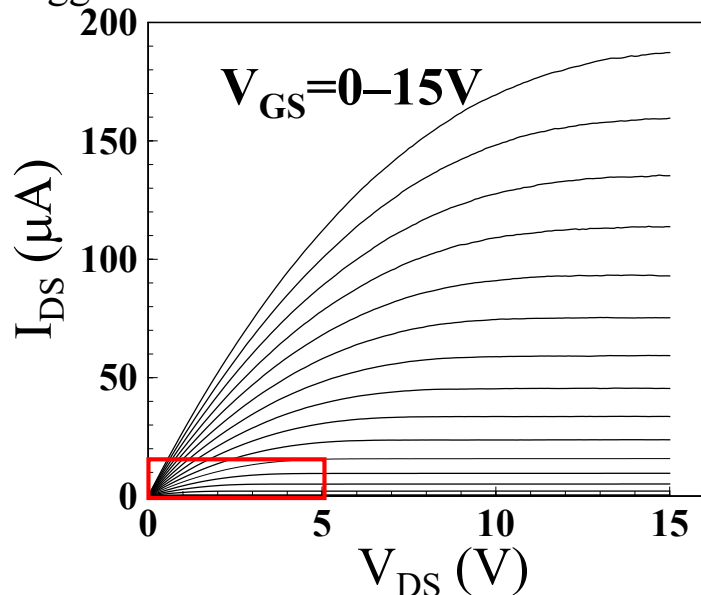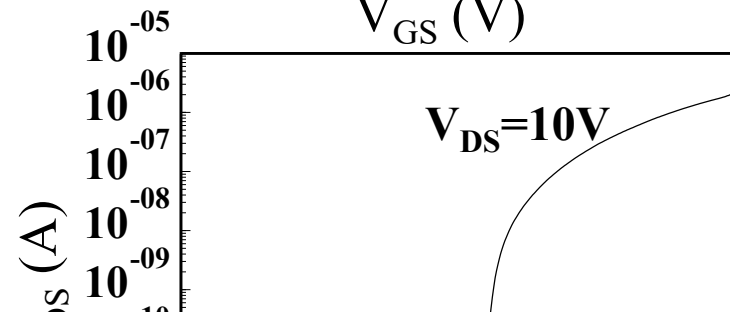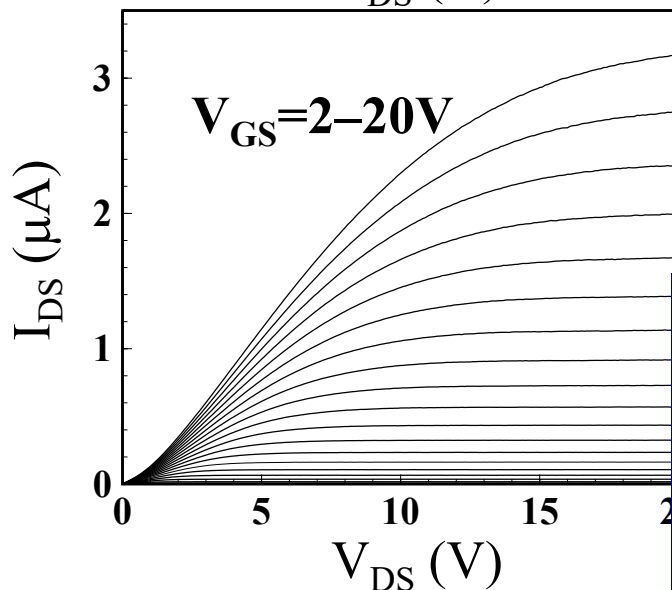
Large on-current

a-InGaZnO$_4$ TFT

$V_{DS} = 4$ V

I$_{DS}$ (A)

V$_{GS}$ (V)
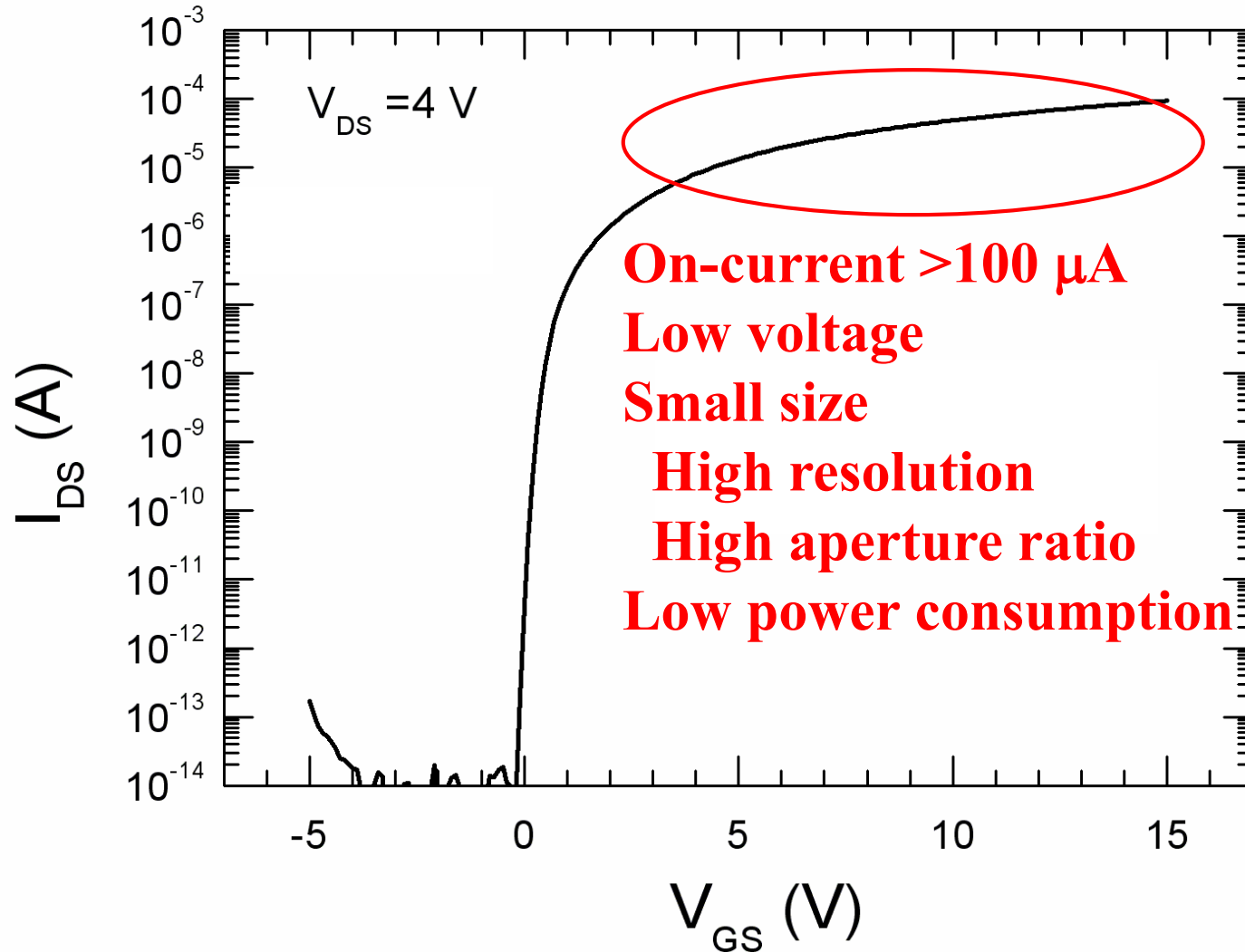
On-current >100 μA
Low voltage
Small size
  High resolution
  High aperture ratio
Low power consumption

Sub-threshold voltage swing (S value)

$$S = \frac{dV}{d \log I_{DS}}$$
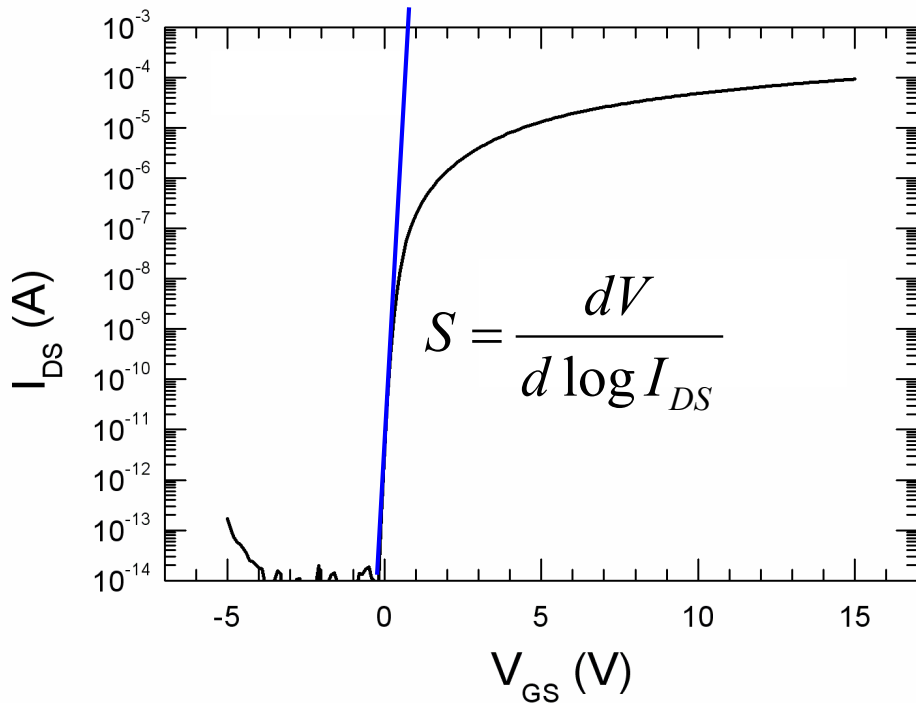
S value

V_{GS} required to increase I_{DS} by an order (@below V_{th})

For a-IGZO
  Small S value: 0.12 V/dec
  Low operation voltages < 5 V

Minimum V_{GS} to switch TFT to on-state: ~ $S \cdot \log I_{ON/OFF}$

  ex.: a-Si:H TFT S = 0.4 V/decade, $I_{ON/OFF}$=10^8 => 3.2 V required

  a-IGZO TFT S = 0.1 V/decade, $I_{ON/OFF}$=10^8 => 0.8 V is enough

Directly related to subgap trap density D_{sg} [(cm²eV)⁻¹]

$$S = \ln 10 \cdot \frac{k_B T}{e} \left(1 + \frac{e D_{sg}}{C_{OX}} \right) > 59\,\text{mV/dec@RT}$$

Advantages of a-IGZO TFT

1. **Large electron mobility** > **10 cm^2/Vs**
2. **Low subgap trap density** (for electron transport)
   Low and wide process temperature: RT–600 ^{o}C
   Low to High operation voltages (1.5 – 100 V)
   Free choice of gate insulator
   Insensitive to metal impurities
3. **Low & flat off-current even for metal contact**
4. **Excellent uniformity and surface flatness**
5. **Large-area mass-production compatible**
   RF / AC / DC sputtering, G8.5 for mass production
6. **Easy fabrication: Owing to the above features**
   Thermal annealing at > 300°C

CONTENT for AOS TFT

IGZO products now

Apple iPad Pro
12.9", 2,732×2,048
(Sharp, LG etc, 2015/11)

Microsoft Surface Pro 4
12.3", 2,736×1,824
(Samsung, 2015/10)

AQUOS EVER SH-02J
5.0", 720×1,280 LCD Full In-Cell
(Sharp, 2016/11/4)

iPad Pro
薄く。軽く。壮大。

Wallpaper TV (OLED)
65" 4K
(LG, 2017/4, in Japan)

OLED TV
88" 8K
(LG, 2018/1, CES2018)
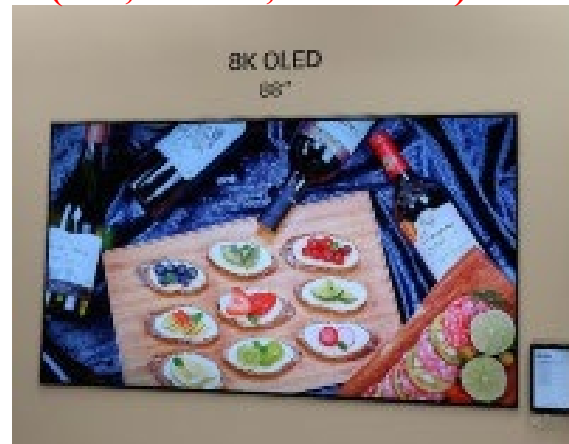
Rollable TV (OLED)
65" 4K
(LG, 2018/1, CES2018)

Large OLED displays

Incheon airport
55" OLED×(10×14), 8×13 m²

N Seoul Tower Plaza (Namsan, Seoul)
OLED 9 m tunnel | **15 m Panorama OLED**

LG 3D World | **Wave OLED ceiling 24 m**

DNP Gotanda Bldg
Show Room
55" OLED×(6×4),
5×4.2 m²
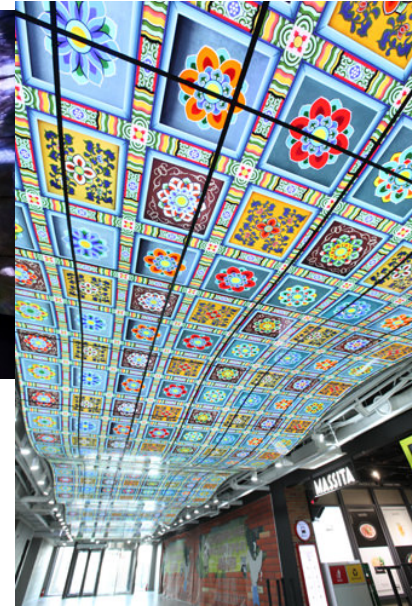
LG (IMID2016)
OLED
Dual-view Curved Tiling
111" 4K, 1500R

Why LG gets success for large OLED?

Sony/Samsung/Everdisplay/Visionox
RGB OLED / LTPS (mc-Si) TFT
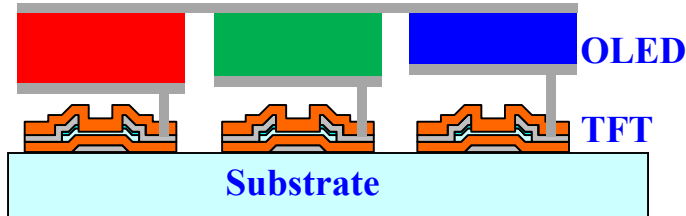
LG
WOLED + WRGB Color Filter
IGZO TFT
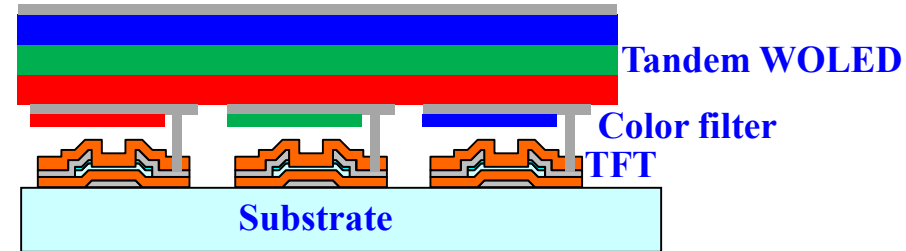
	Smart phone to Note PC (15")	Desktop 27" to Large TV (up to 77")		
TFT	P-ch LTPS TFT	N-ch Oxide TFT		
OLED	RGB side by side Top emission Normal structure	WOLED / RGB CF Bottom emission Normal structure		
Pixel compensation	**Several TFTs (~ 8Tr in Galaxy)**	Several TFTs	**3 TFTs**	
External compensation			**Real-time sensing Memory IC**	

Low and flat off-current in a-IGZO TFT

a-InGaZnO$_4$ TFT

No inversion, Low off current irrespective of metal / a-IGZO contacts
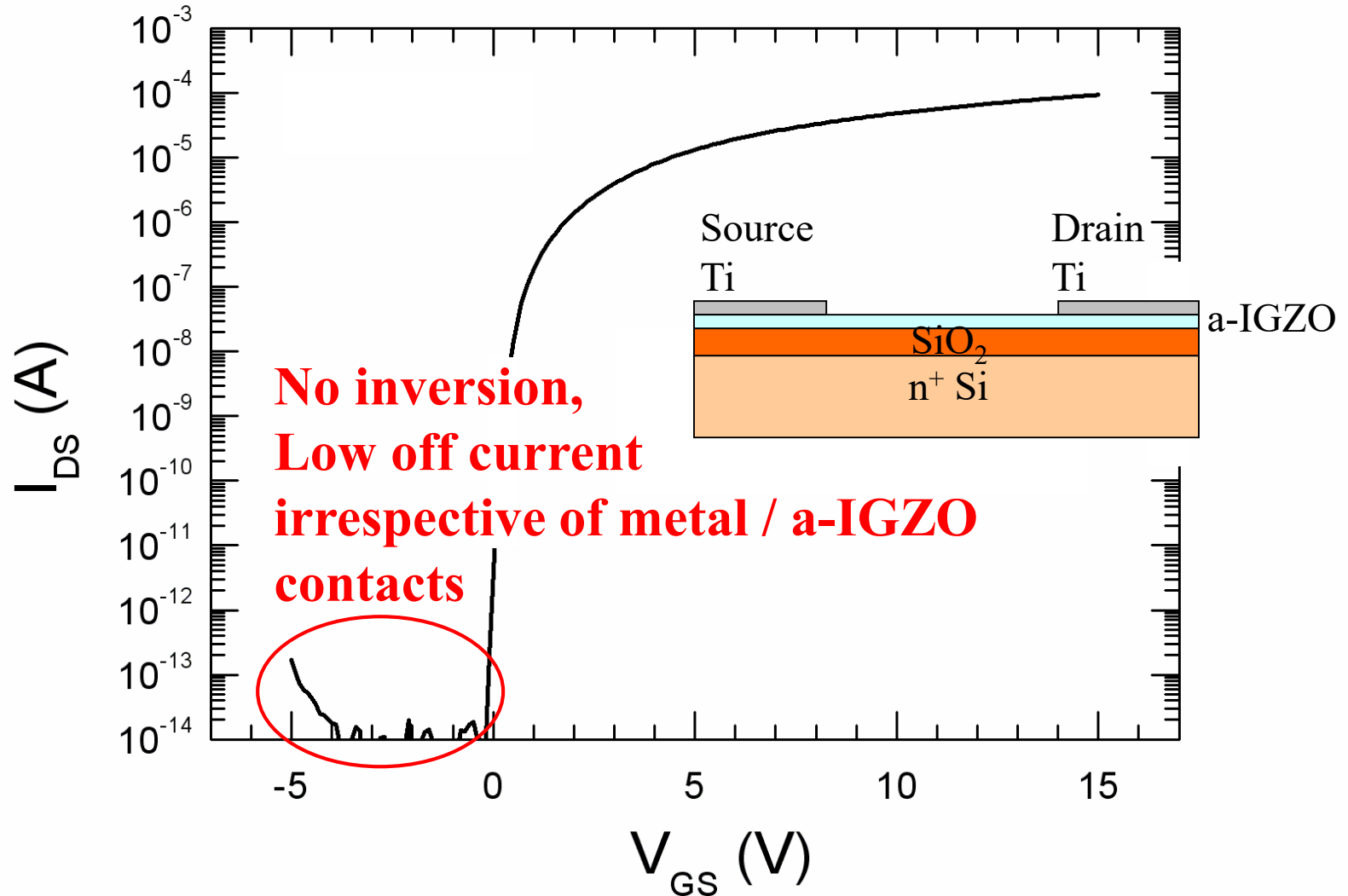
Very low & flat off current in IGZOTFTs

CAAC IGZO:

T. Tanabe et al, AM-FPD2011, P-7

K. Kato et al., Jpn. J. Appl. Phys. **51** (2012) 021201

H. Inoue et al, IEEE J. Solid-State Circuits **47** (2012) 2258

S. Yamazaki et al., Jpn. J. Appl. Phys. **53** (2014) 04ED18

I_{off}: ~10^{-23} A/μm at 85°C   ~10^{-25} A/μm at 27°C
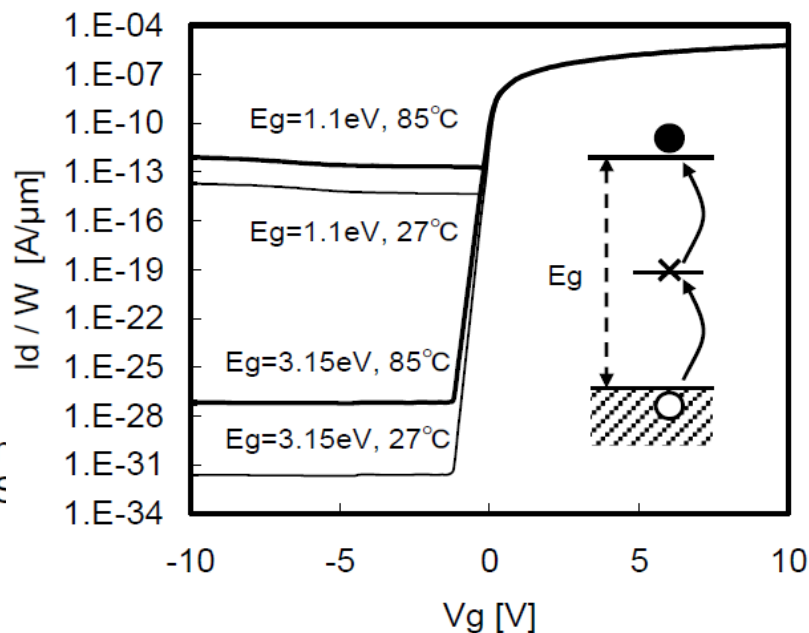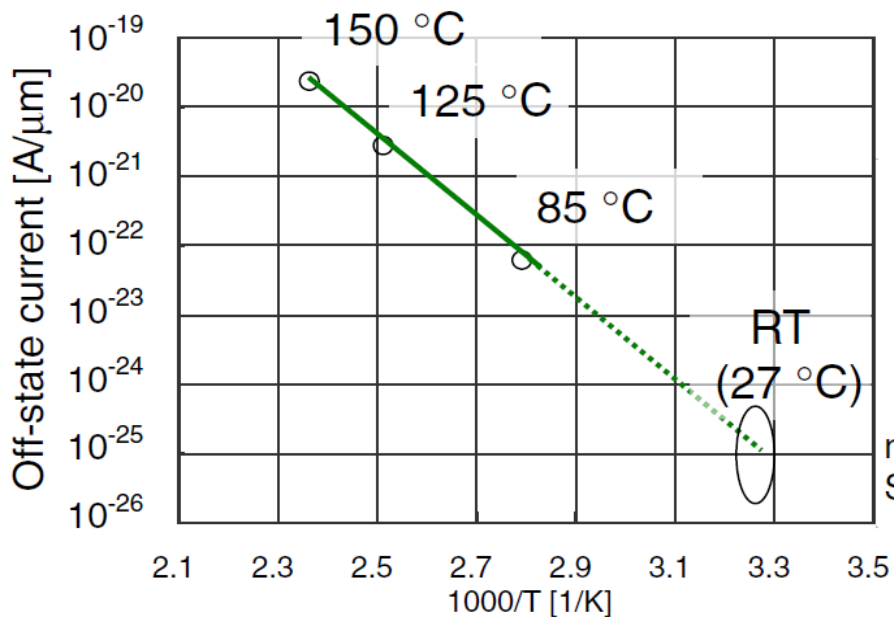
Conventinal IGZO TFT annealed at 350°C in Ar:

Y. Yamauchi, Y. Kamakura, Y. Isagi, T. Matsuoka, S. Malotaux,
  Jpn. J. Appl. Phys. **52**, 094101 (2013)

I_{off}: 2.8×10^{-20} A/μm at 60°C

LCD idling stop in IGZO LCDs

Sharp http://www.sharp.co.jp/products/sh02e/
SID 2013, 56

a-Si TFT
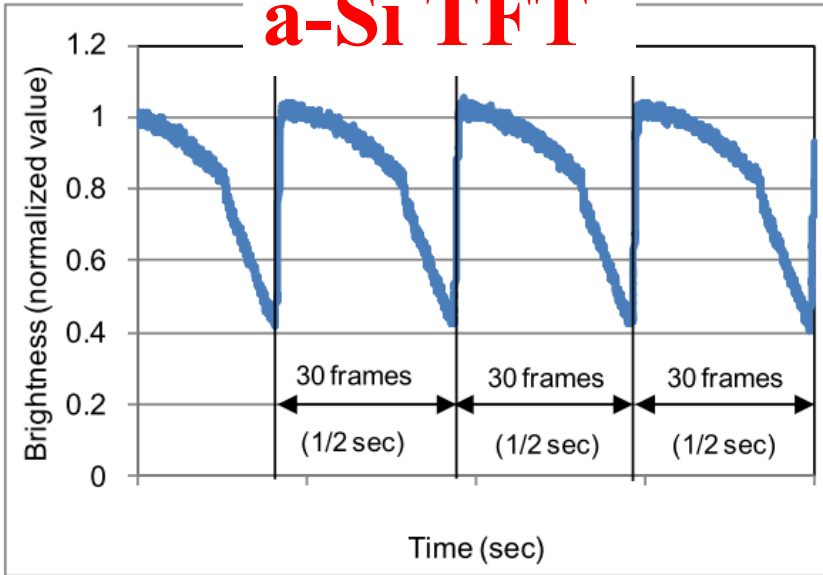
IGZO TFT

■ 静止画表示時の使用電力

a-Si — always ON
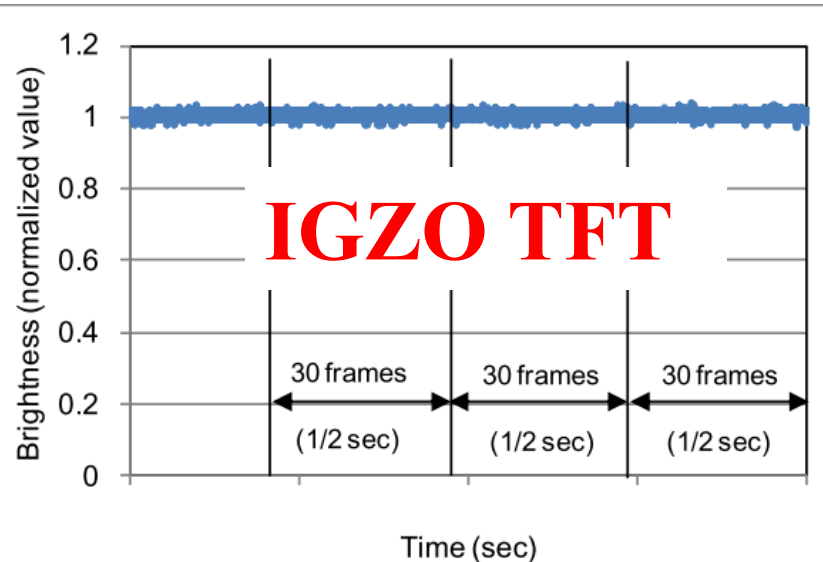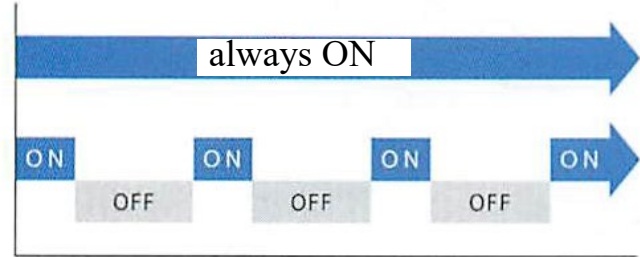
❄IGZO — ON / OFF / ON / OFF / ON / OFF / ON

■ Comparison

	IGZO	a-Si
	SH-02E	SH-01D (2011冬)
Lasting time (picture)	~24 h, ×4.8	~5 h
Lasting time (movie)	~11 h, ×2.8	~4 h

Sharp@SID2014:
Back light:
245mW@200cd/m²

Capacitive touch pen
With SH-02E Conventional

60 Hz, TFT, Back light, 1 Hz — Power consumption (mW)
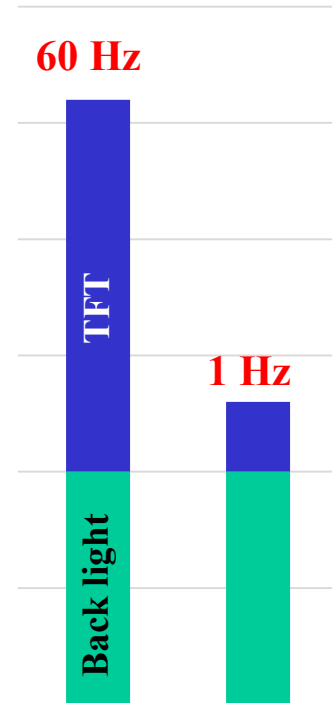
Flexible displays using oxide TFTs

**a-IGZO, Organic ESL
12.1" 1,280×800, TN LCD
(AUO, IDW2013)**
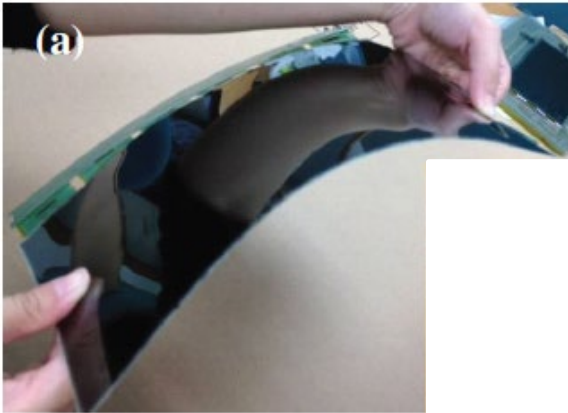
**Transfer technology, WOLED+CF
10.2" WUXGA OLED
(Toshiba, IDW2013)**

**Transfer technology, WOLED+CF
13.5" 4K OLED
(SEL/AFD/Sharp, AMFPD'13)**

**Side-/Top-roll panels
Transfer technology, WOLED+CF
(SEL/Nokia, SID2014)**

**Tri-foldable OLED
Transfer technology, WOLED+CF
(SEL, SID2014)**

**Solution & Flexible
T_{max} = 250°C, μ = 2.17 cm^2/Vs
(IMEC, IDW11)**
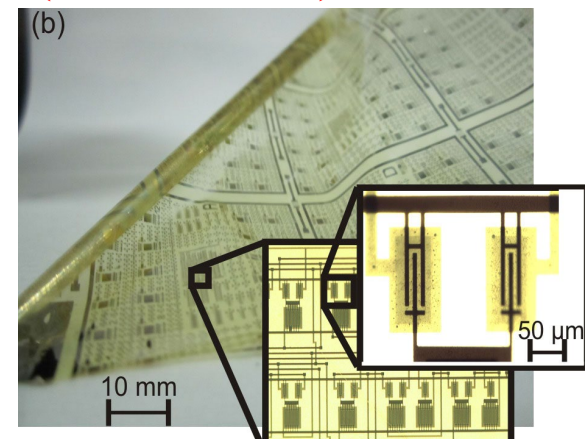
CONTENT for AOS TFT

1. Characteristics of a-IGZO TFT
2. Current AOS displays
3. **Materials**
4. Growth condition and TFT fabrication
5. Doping
6. Defect structures (subgap defects)
7. Why too large P_{O2} is bad?:
           Weakly-bonded Oxygen
8. Annealing
9. Hydrogen

InGaZnO$_4$

Crystal InGaZnO$_4$

O
In
Zn,
Ga

a-InGaZnO$_4$

Single-crystalline InGaO$_3$(ZnO)$_5$

00021
0000

[0001]
[1120]

2nm

80cm^2/Vs

V$_{GS}$ (V)

10
9
8
7
6
< 5

Drain current, I$_{DS}$ (mA)

Drain voltage, V$_{DS}$ (V)

10cm^2/Vs

V$_{GS}$ (V)

6.0
5.0
4.0
3.0
2.0
1.0

Drain current, I$_{DS}$ (mA)

Drain voltage, V$_{DS}$ (V)

a-InGaZnO$_4$

3nm
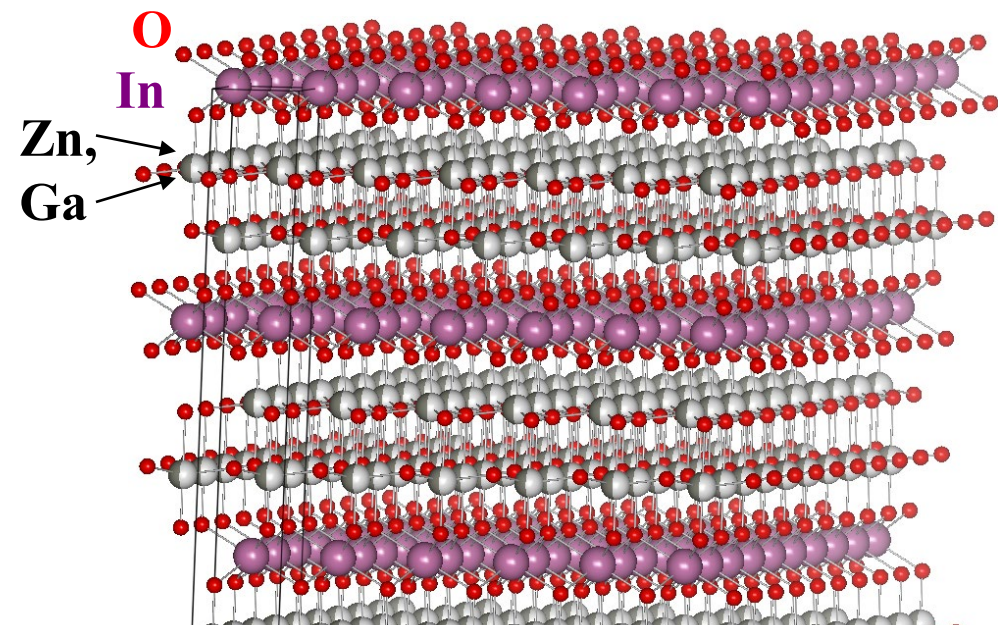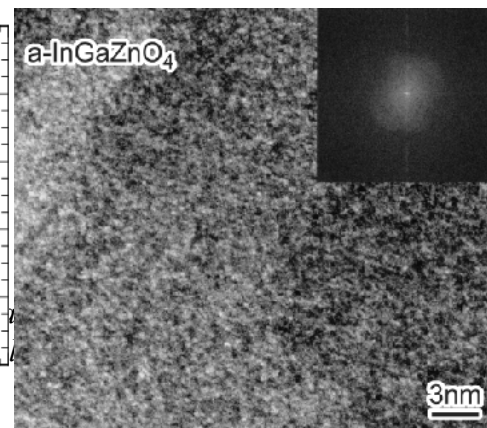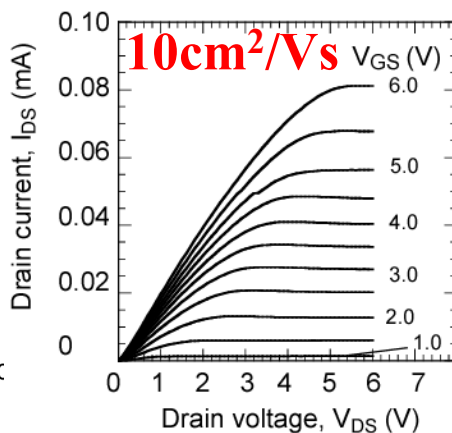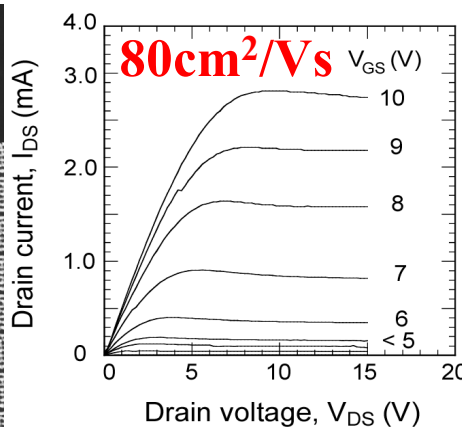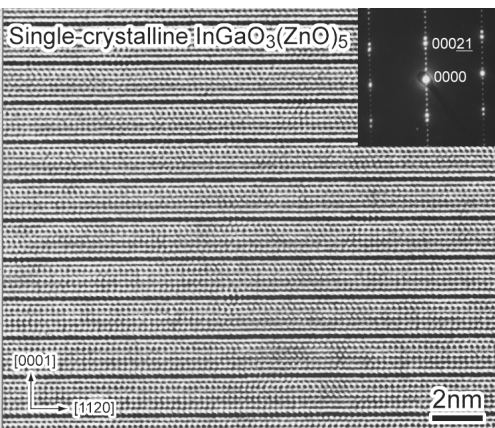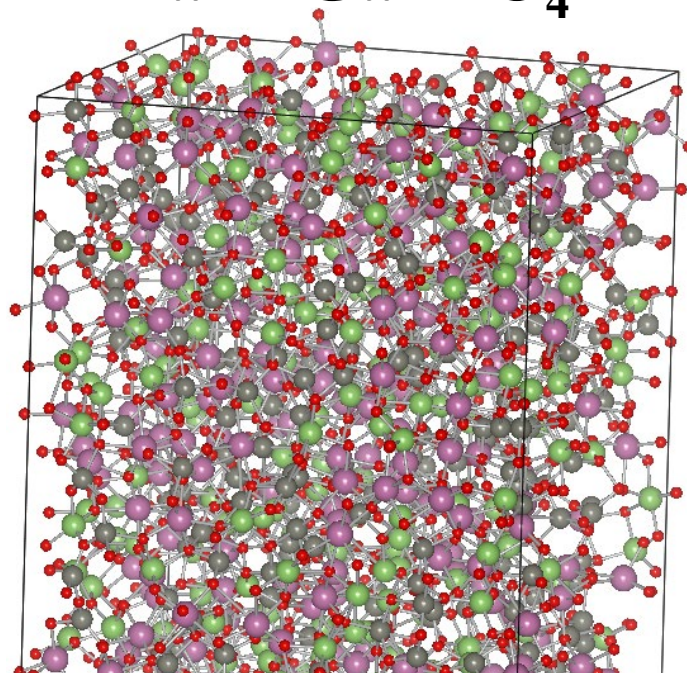
Elements reported for AOSs

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Ia	IIa	IIIa	IVa	Va	VIa	VIIa		VIII		Ib	IIb	IIIb	IVb	Vb	VIb	IIb	0
H 1																	He 2
Li 3	Be 4											B 5	C 6	N 7	O 8	F 9	Ne 10
Na 11	Mg 12											Al 13	Si 14	P 15	S 16	Cl 17	Ar 18
K 19	Ca 20	Sc 21	Ti 22	V 23	Cr 24	Mn 25	Fe 26	Co 27	Ni 28	Cu 29	Zn 30	Ga 31	Ge 32	As 33	Se 34	Br 35	Kr 36
Rb 37	Sr 38	Y 39	Zr 40	Nb 41	Mo 42	Tc 43	Ru 44	Rh 45	Pd 46	Ag 47	Cd 48	In 49	Sn 50	Sb 51	Te 52	I 53	Xe 54
Cs 55	Ba 56	*Ln	Hf 72	Ta 73	W 74	Re 75	Os 76	Ir 77	Pt 78	Au 79	Hg 80	Tl 81	Pb 82	Bi 83	Po 84	At 85	Xe 86
Fr 87	Ra 88	**Ac	Rf 104	Db 105	Sg 106	Bh 107	Hs 108	Mt 109	Ds 110	Rg 111	Cn 112	Uut 113	Uuq 114	Uup 115	Uuh 116	Uus 117	Uuo 118

Typical AOS: In – Zn – Sn – Ga – O
Constituents of
known Transparent Conductive Oxides:
In_2O_3, SnO_2, ZnO, Ga_2O_3
$MgIn_2O_4$ etc. (TiO_2)

STO orbital radius

	IIb	IIIb	IVb
3		Al^{3+} 113 pm	Si^{4+} 92 pm
4	Zn^{2+} 154 pm	Ga^{3+} 127 pm	Ge^{4+} 108 pm
5	Cd^{2+} 180 pm	In^{3+} 149 pm	Sn^{4+} 126 pm

AOS materials

General trend

Mobility increases with In ratio (mobility enhancer) ⇔ Negative V_{th} shidt

Mixing different ions stabilizes amorphous structure. (Zn: network stabilizer)

Ga suppresses formation of oxygen deficiency (stabilizer/suppressor)

a-In-Ga-Zn-O (a-IGZO) (2004 Tokyo Tech)

In : Ga : Zn = 1 : 1 : 1 (Korean groups 2 : 2 : 1)

C-Axis Aligned Crystal (CAAC) (SEL)

Zn-Sn-O (ZTO), Zn-In-O (ZIO) (2005 OSU & Hewlett-Packard)

20~55 cm^2/Vs, 300~600° annealing

10wt% ZnO doped a-In_2O_3 (IZO) (Idemitsu): >50 cm^2/Vs @ N_e >> 10^{20} cm^{-3}

Stabilizer: Al, Mg, Si, Hf

Mobility sharply decreases at the stabilizer conc. > 3 – 5%

In-Ga-O (IGO) (OSU&HP)

Al-Zn-Sn-O (AZTO), Al-Sn-In-Zn-O (ETRI)

Hf-In-Zn-O (HIZO) (Samsung Advanced Institute of Technology (SAIT))

In-Sn-Zn-O (ITZO), c-In-Ga-O (c-IGO) (Sony&Idemitzu)

c-Zr-In-Zn-O (Samsung SDI)

a-Zn(O,N) (Appl. Mater, SAIT)

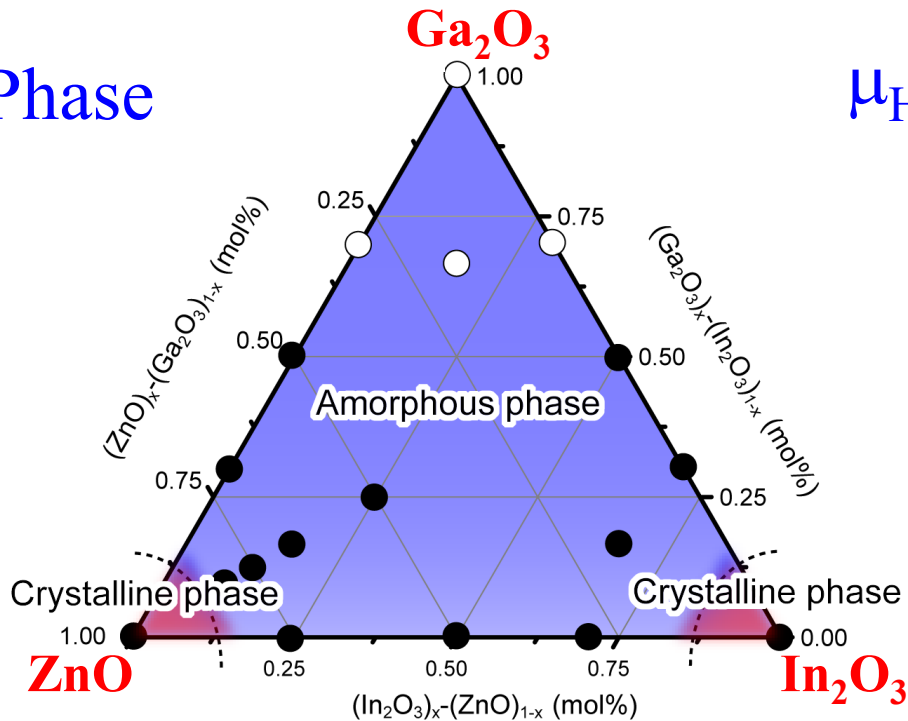**In-Al-Zn-O** (CBRITE)

In-W-O, In-Si-O (NIMS)

Chemical composition mapping

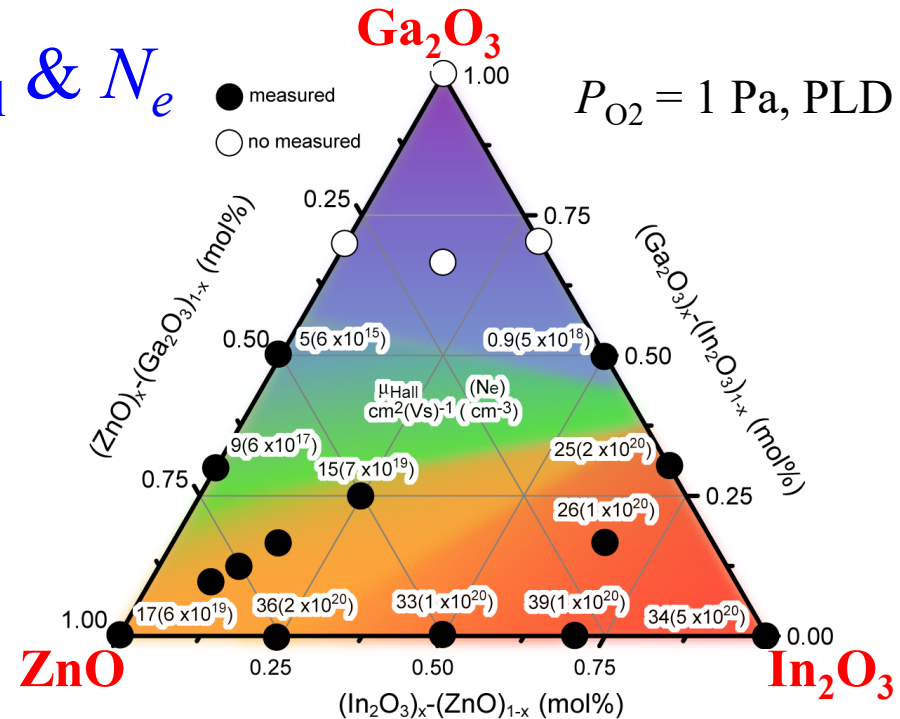**Multi-component metal oxides** (different ion charges / sizes)
Deposition @ RT (sputtering, PLD)
Amorphous phase stable up to ~500ºC for a-InGaZnO$_4$

Phase

Ga$_2$O$_3$

$(ZnO)_x$-$(Ga_2O_3)_{1-x}$ (mol%)

$(Ga_2O_3)_x$-$(In_2O_3)_{1-x}$ (mol%)

Amorphous phase

Crystalline phase

Crystalline phase

ZnO

In$_2$O$_3$

$(In_2O_3)_x$-$(ZnO)_{1-x}$ (mol%)

μ_{Hall} & N_e

Ga$_2$O$_3$

P_{O2} = 1 Pa, PLD

● measured
○ no measured

$(ZnO)_x$-$(Ga_2O_3)_{1-x}$ (mol%)

$(Ga_2O_3)_x$-$(In_2O_3)_{1-x}$ (mol%)

5(6 x10^{15})   0.9(5 x10^{18})

μ_{Hall} (N_e)
cm^2(Vs)$^{-1}$ (cm^{-3})

9(6 x10^{17})

15(7 x10^{19})   25(2 x10^{20})

26(1 x10^{20})

17(6 x10^{19}) 36(2 x10^{20}) 33(1 x10^{20}) 39(1 x10^{20}) 34(5 x10^{20})

ZnO

In$_2$O$_3$

$(In_2O_3)_x$-$(ZnO)_{1-x}$ (mol%)

In$_2$-Zn$_3$-O (IZO)   : ~40 cm^2(Vs)$^{-1}$
In-Zn-Ga-O (IGZO) : ~26 cm^2(Vs)$^{-1}$
In$_3$-Ga$_7$-O (IGO)   : ~25 cm^2(Vs)$^{-1}$
Zn$_3$-Ga$_{14}$-O (ZGO)   : ~10 cm^2(Vs)$^{-1}$

General mobility and carrier concentration relationship in transparent amorphous indium zinc oxide films

A.J. Leenheer et al., *Phys. Rev. B 77, 115215 2008*

a-IZO (10wt%ZnO-In$_2$O$_3$)
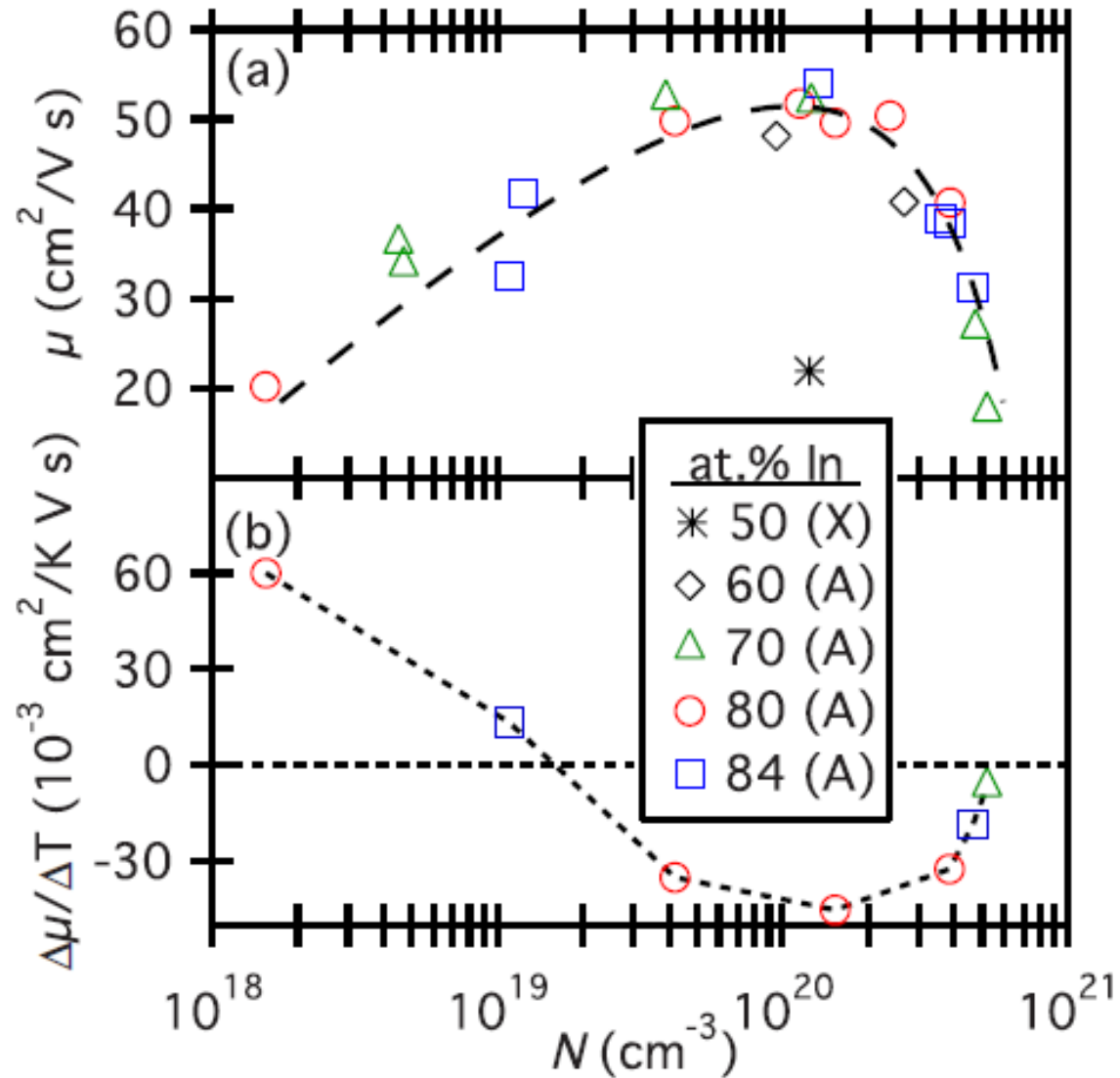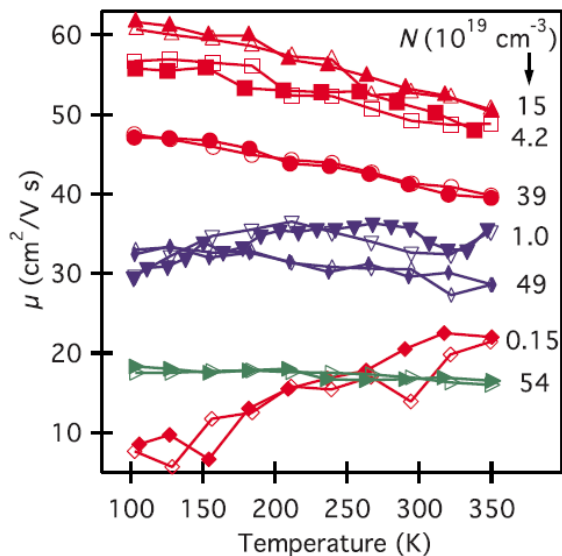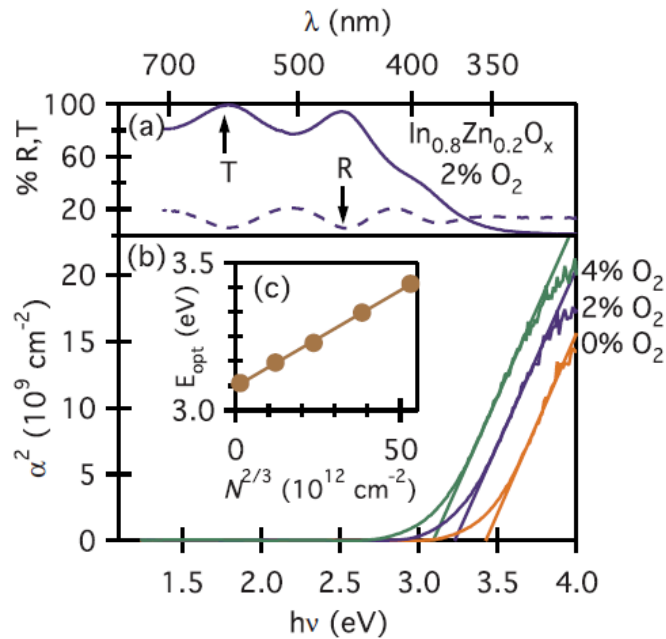
In-Sn-Zn-O (ITZO)

SID2014 **53.1**

AMFPD2014 **SP-3 AUO**

  High mobility metal oxide thin film transistors

  active-matrix organic light-emitting diode television

    G6, TFT mobility ~33.2 cm^2/Vs, OLED: RGB SBS/FMM
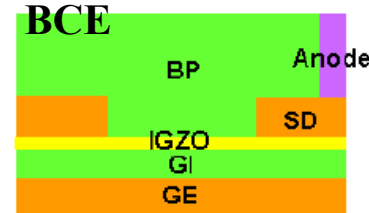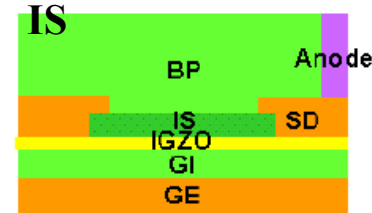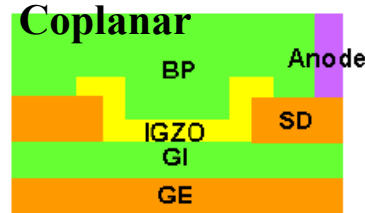
    14" qHD a-IGZO / 32" FHD a-IGZO / 65" FHD a-IGZO

    56" IS type a-ITZO / **56" BCE type a-ITZO** / 65" FHD a-ITZO

AMFPD2014 **S1-2 KAIST/ETRI**

  Back channel etch oxide TFT on plastic substrate

  for the application of high resolution TFT-LCD

  Al-ZnSnInO BCE TFT

SID2013 56.2   AUO   : IGZO 65" 4K OLED
SID2013 21.3   AUO   : IGZO 65" FHD OLED
IDW2013 OLED5-4L AUO   : a-IGZO 56" OLED
IDW2013 AMD2-1   AUO   : oxide (IGZO?) 65" FHD OLED
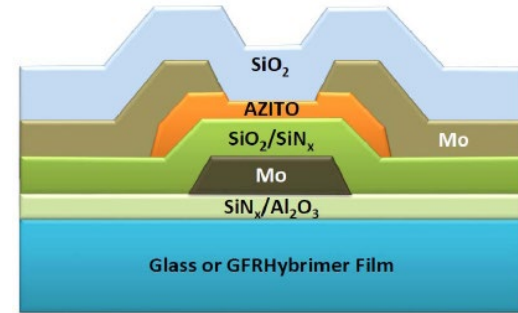薄膜材料デバイス研究会2012 2O03 高知工科大: ITZO **depo@150ºC, ann@350ºC in N$_2$**
SID2012 74.1L   Sony   : IGZO Flexible 9.9" 960×540 2Tr AMOLED
SID2012 56.1   Sony   : Comparison IGZO vs ITZO vs a-Si
AMFPD2011 7-1   Idemitzu   : Etching rate of a-ITZO, a-IGZO, a-ITO, a-IZO
IDW2010 AMD5/OLED6-2 Sony: a-ITZO 8" 1600×768 (221ppi) 2T1C AMOLED (WRGB)

a-Zn(O,N)

X.-A. Zhang et al., TSF **516**, 3305 (2008): N-doped crystalline ZnO, μ_{FE} = 2.7 cm^2/(Vs)

Y. Ye et al. (Appl. Mater.), JAP 106, 074512 (2009):

μ_{Hall} = 110 cm^2/(Vs) (400°C anneal), μ_{sat} = 10 cm^2/(Vs) (350°C anneal)

J.S. Park et al. (SAIT), IDW/AD'12, AMD3-4:

(Zn,Ga)(O,N) μ_{FE} = 92 cm^2/(Vs) (350°C anneal), **N-rich => larger mobility**

M. Ryu et al. (SAIT), IEDM12 5.6: Zn(O,N) μ_{FE} = 100 cm^2/(Vs) (250°C anneal)

H.-S. Kim et al. (SAIT), Sci. Repts. 3, 1459 (2013)
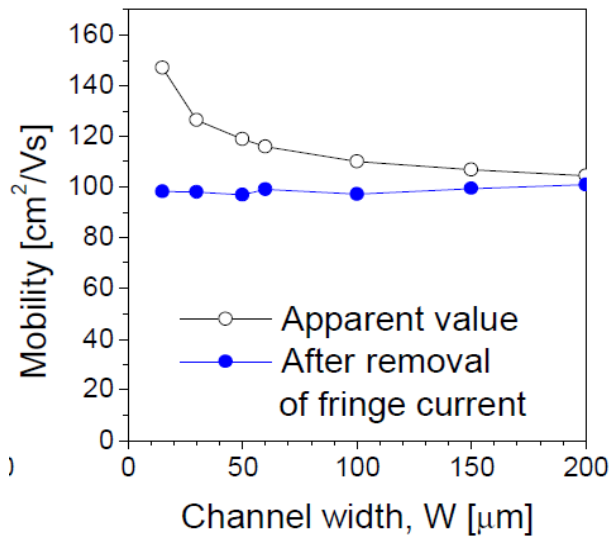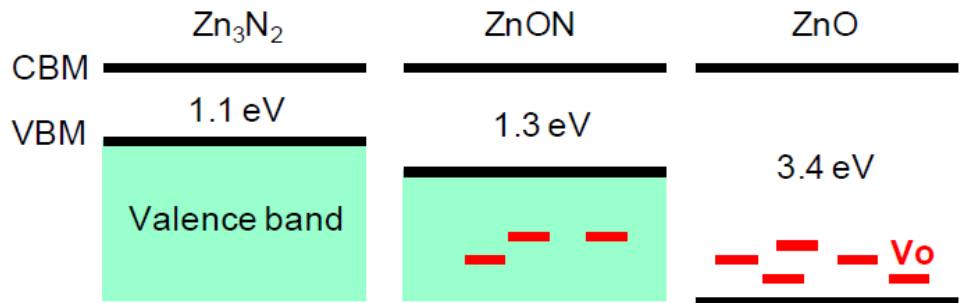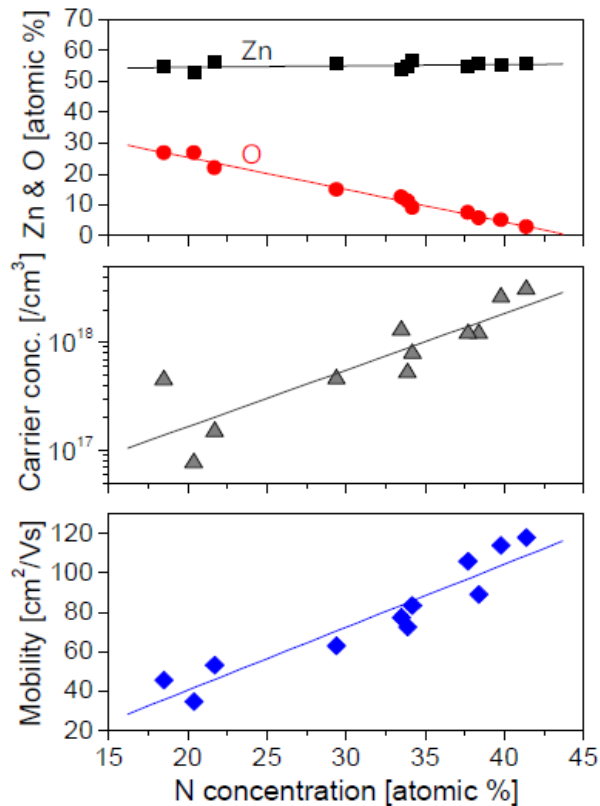
Amorphous ZnO_xN_y Thin Films with Mobilities Exceeding 200 cm²V⁻¹s⁻¹

T. Yamazaki, K. Shigematsu, Y. Hirose, S. Nakao, I. Harayama, D. Sekiba, T. Hasegawa

PLD, ZnO target
N radical by ECR source
Glass substrate
Growth rate 0.4-0.7 nm/min

N increase => N_e decrease
**   => μ increase**
$μ_{Hall}$ up to 240 cm²/(Vs)
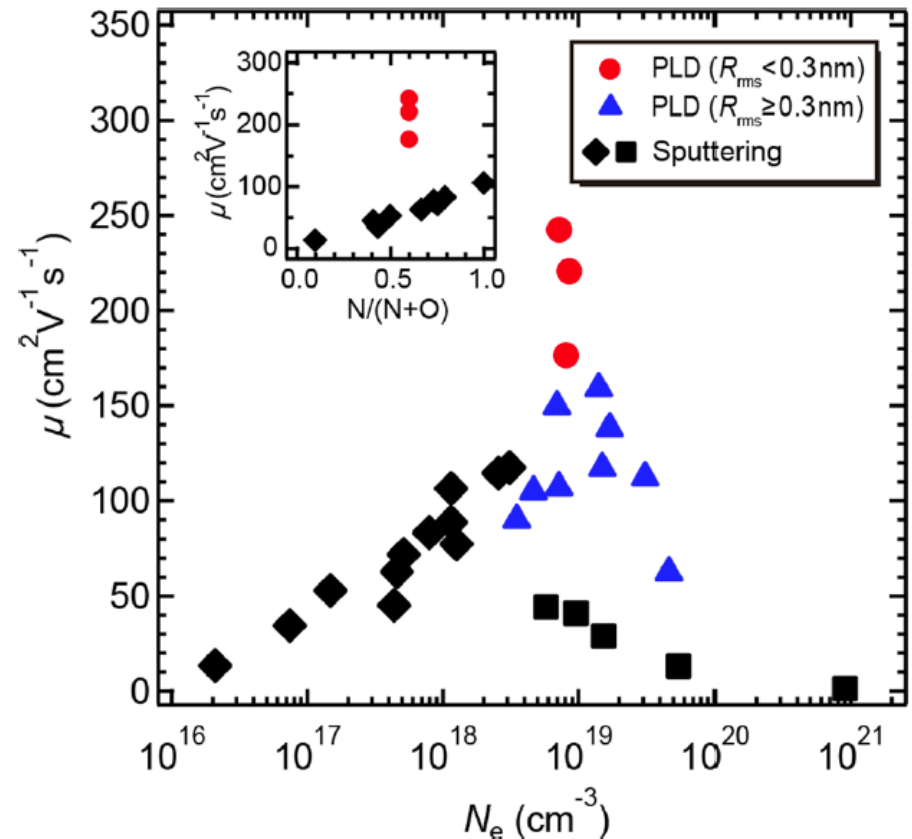
Electrical Properties of the Thin-Film Transistor With an Indium–Gallium–Zinc Oxide Channel and an Aluminum Oxide Gate Dielectric Stack Formed by Solution-Based Atmospheric Pressure Deposition

Mamoru Furuta, Toshiyuki Kawaharamura, Dapeng Wang,
Tatsuya Toda, and Takashi Hirao
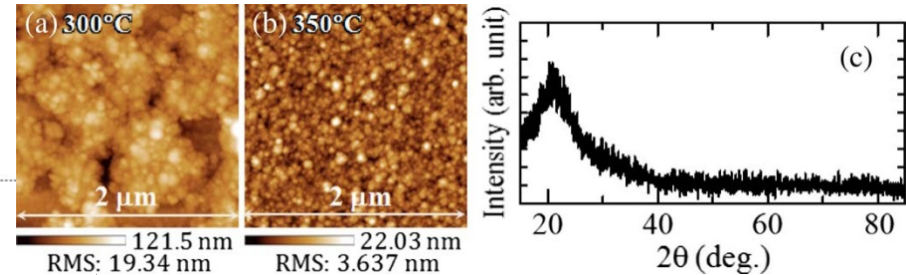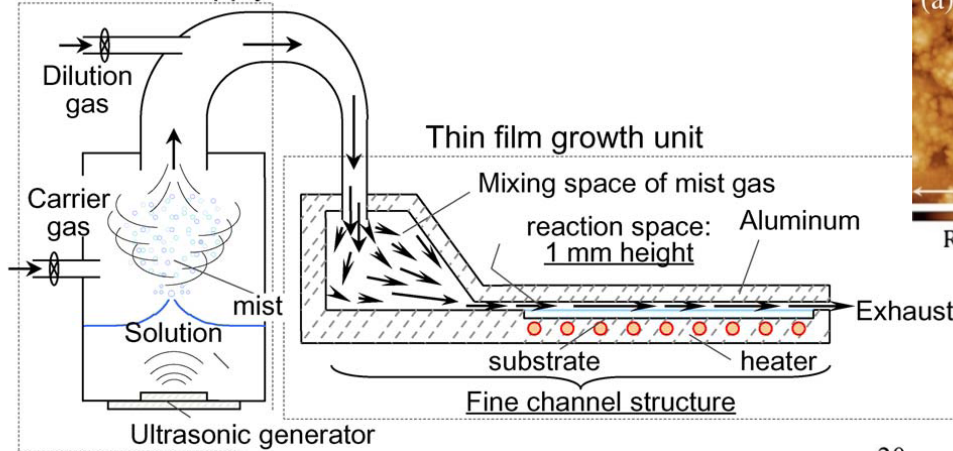
200-nm-thick IGZO films deposited at (a) 300 C and (b) 350 C on a-SiO$_2$

Mist-CVD

Atmospheric pressure

Al$_2$O$_3$: 0.02 M Al(acac) [acetylacetonate]
@300-430°C

IGZO: In(acac), Ga(acac), Zn(acac)
@300-350°C
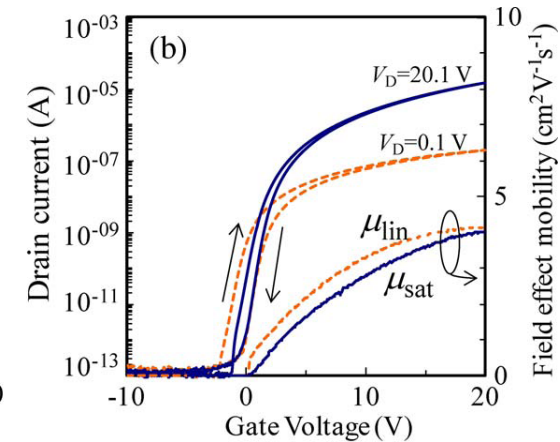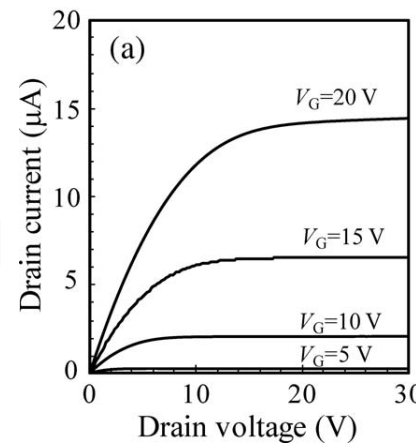
μ_{lin} = 4.2 cm²/Vs

μ_{sat} = 4 cm²/Vs

CONTENT for AOS TFT

1. Characteristics of a-IGZO TFT
2. Current AOS displays
3. Materials
4. **Growth condition and TFT fabrication**
5. Doping
6. Defect structures (subgap defects)
7. Why too large P_{O2} is bad?:
   Weakly-bonded Oxygen
8. Annealing
9. Hydrogen

Simple fabrication of a-IGZO TFT

1. **Buy Si wafer (150nm SiO$_2$)**
2. **Pattern a-IGZO**
3. **Anneal @ 400ºC air / O$_2$(+H$_2$O)**
4. **Pattern S/D**
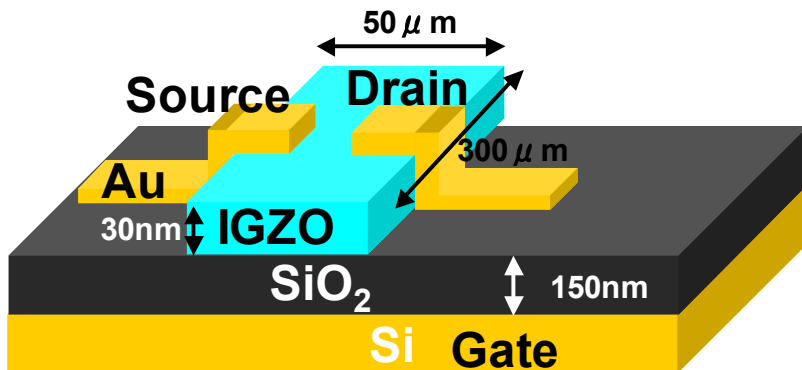
a-IGZO thickness：30nm (Wet annealed)
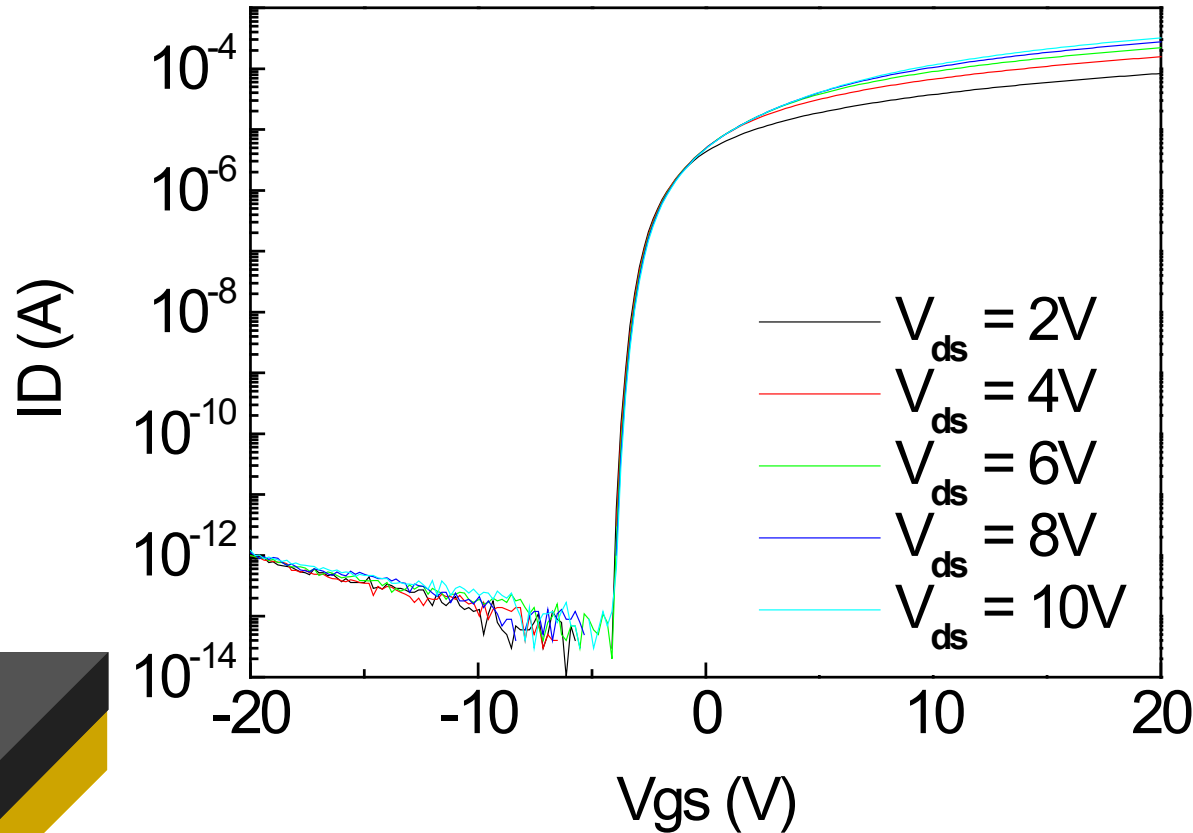
S = 0.12 V/decade

V$_{th}$ = -2.58 V

μ$_{sat}$ = 15.3 cm^2/Vs

Recipe of a-IGZO TFT for beginners

1. Fabricate/Buy sputtering target: $In_2O_3 : Ga_2O_3 : ZnO = 1 : 1 : 2$

(Note: In: Ga: Zn = 1: 1: 1)

* 1:1:1 in 'the chemical formula unit' composition is also used,
  but we recommend '1:1:1 in the atomic composition.'

2. Deposit 30 – 50 nm thick (~70 nm for large-area products)
a-InGaZnO$_4$ on ~100nm SiO$_2$ / n$^+$ c-Si wafer at RT
($\sigma = 10^{-3} – 10^{-6}$ Scm^{-1})

* Substrate heating is not necessary (may be crystallized at >180°C)
* Channel regions should be isolated
    suppress gate leakage current, improve S value,
    can avoid to observe apparent large mobility
* Deposition condition (RF power, P_{O2} etc) is not critical
* Low purity/vacuum deposition system can be used

3. Annealed in air / O$_2$ at 300 – 400 ^{o}C

* Better not to form source/drain electrode at this stage

4. Form source/drain top contacts with Ti, (Au,Al)/Ti, ITO, etc

* P/N junction is not necessary (No inversion operation for a-IGZO TFTs)

a-IGZO is clean?

Yes, near CBM
But can be dirty in the deep half E_g
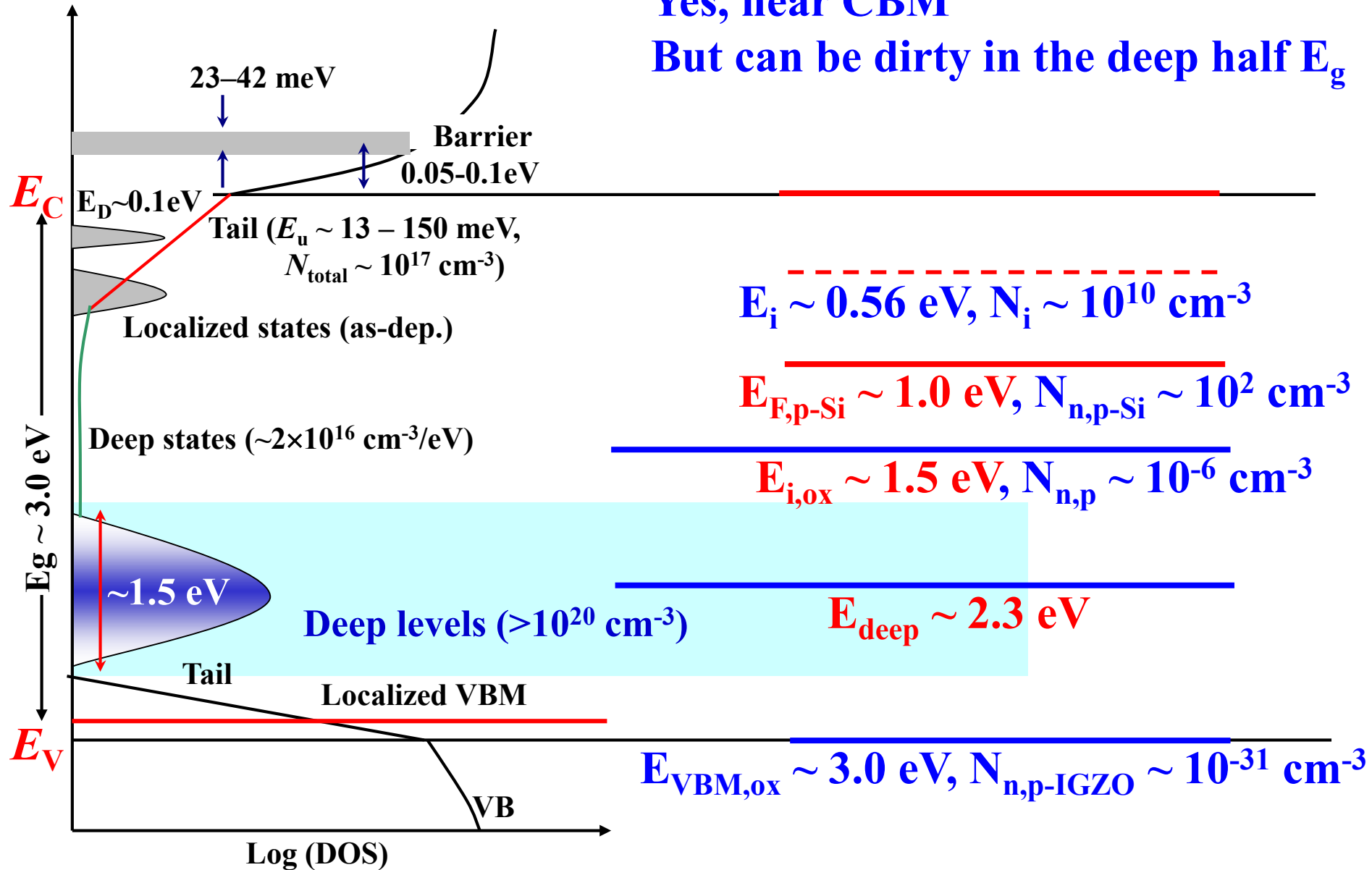
23–42 meV

$E_D \sim 0.1$ eV

Barrier
0.05-0.1eV

E_C

Tail ($E_u \sim 13 - 150$ meV, $N_{total} \sim 10^{17}$ cm^{-3})

Localized states (as-dep.)

Deep states (~2×10^{16} cm^{-3}/eV)

$E_i \sim 0.56$ eV, $N_i \sim 10^{10}$ cm^{-3}

$E_{F,p\text{-Si}} \sim 1.0$ eV, $N_{n,p\text{-Si}} \sim 10^2$ cm^{-3}

$E_{i,ox} \sim 1.5$ eV, $N_{n,p} \sim 10^{-6}$ cm^{-3}

~1.5 eV

Deep levels (>10^{20} cm^{-3})

$E_{deep} \sim 2.3$ eV

Tail

Localized VBM

E_V

$Eg \sim 3.0$ eV

VB

Log (DOS)

$E_{VBM,ox} \sim 3.0$ eV, $N_{n,p\text{-IGZO}} \sim 10^{-31}$ cm^{-3}

Optimum oxygen pressure

Good TFTs:

$N_D = 10^{12} - 10^{15}$ cm^{-3}

$\sigma = 10^{-6} - 10^{-3}$ Scm^{-1}
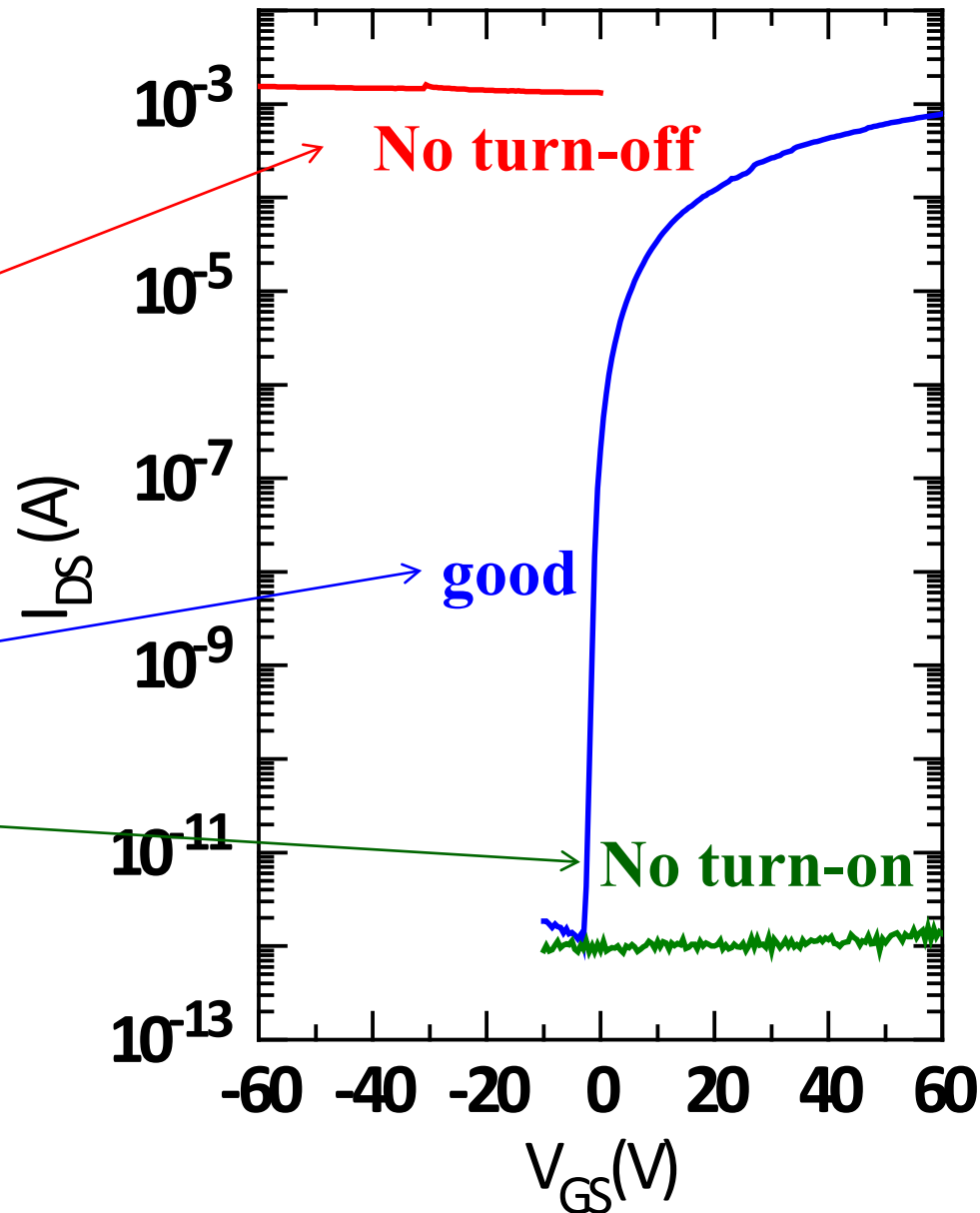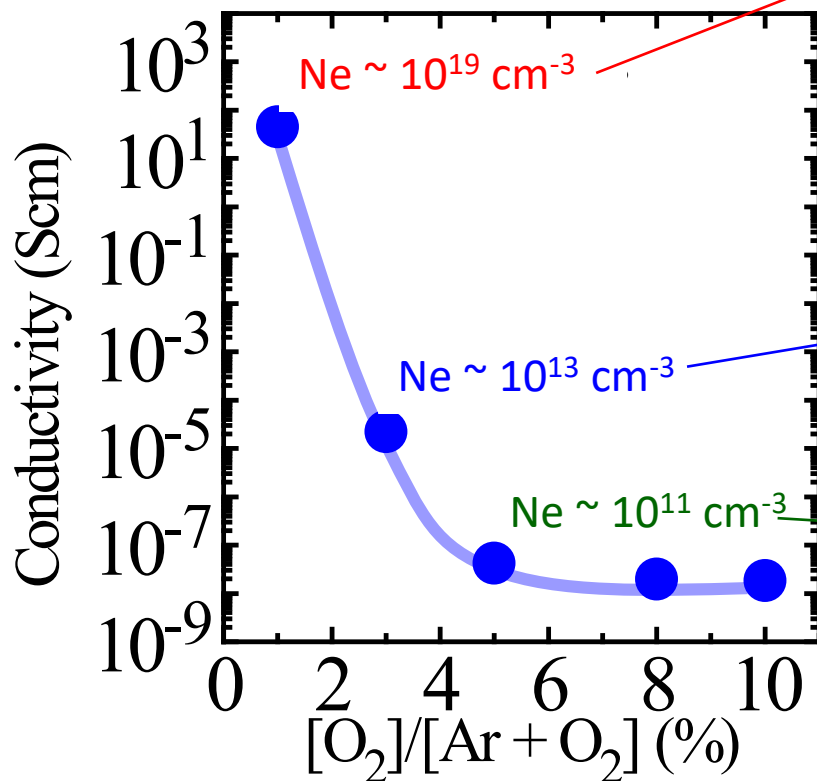
Trend of optimum deposition condition

1. **Substrate temperature <180°C**
   Crystal growth occurs at higher T.
   ~100°C is better for stable reproducibility?
2. **Large ion bombardment condition**
   High-rate growth
   High power
   Low working pressure (P_{tot})
   Small Target-Substrate distance
   Low-T growth requires kinetic energy for structure relaxation.
   Increase film density (Ion packing density)
   Decrease impurity H
   => Decrease defects
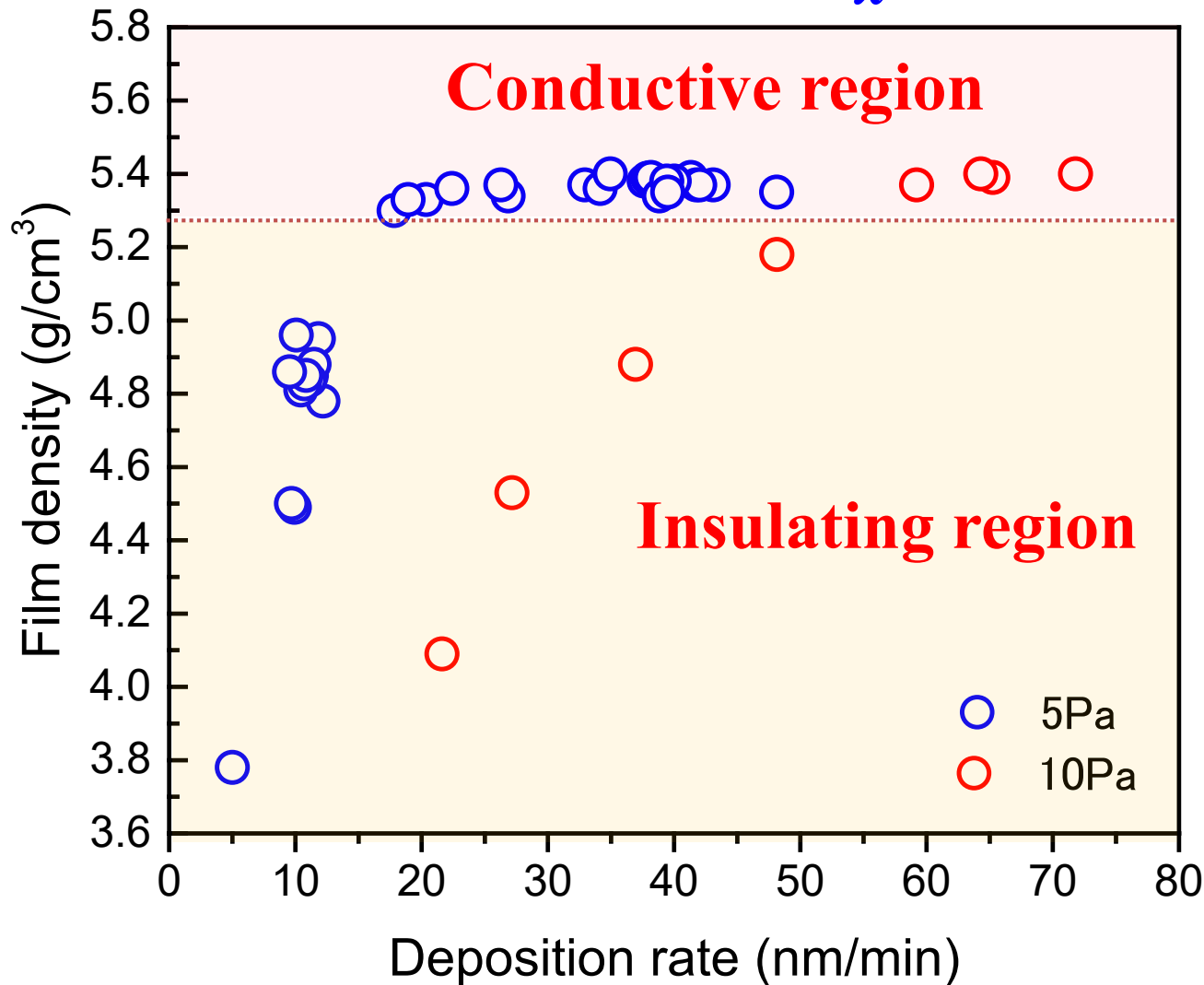3. **Finely tune oxygen partial pressure (P_{O2})**
   => Decrease defects
4. **Post-deposition annealing at $\geq$ 300°C**
   Remove weakly-bonded O and H_2O
   Structural relaxation to increase the film packing density
   O in-diffusion to remove V_O-related defects

High growth rate produces high-density films for a-GaO$_x$

Control of defects: conducting a-Ga₂O₃

Conductivity

Low density Void, OH

Low density Excess O

Transmittance

E_g = 4.12 eV
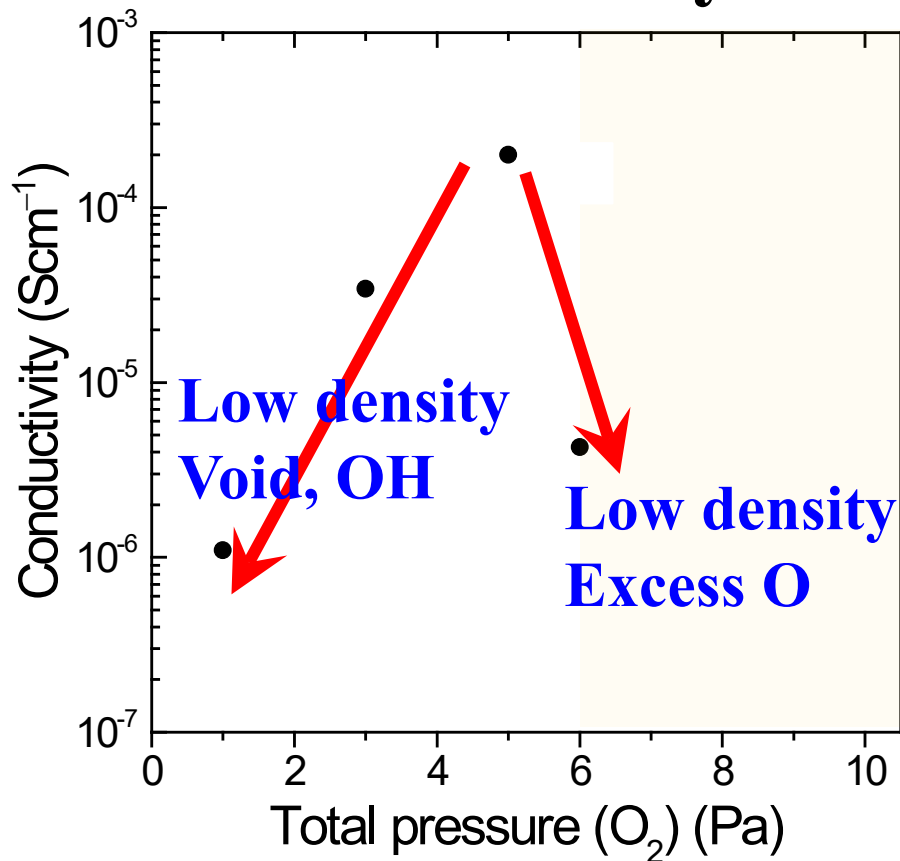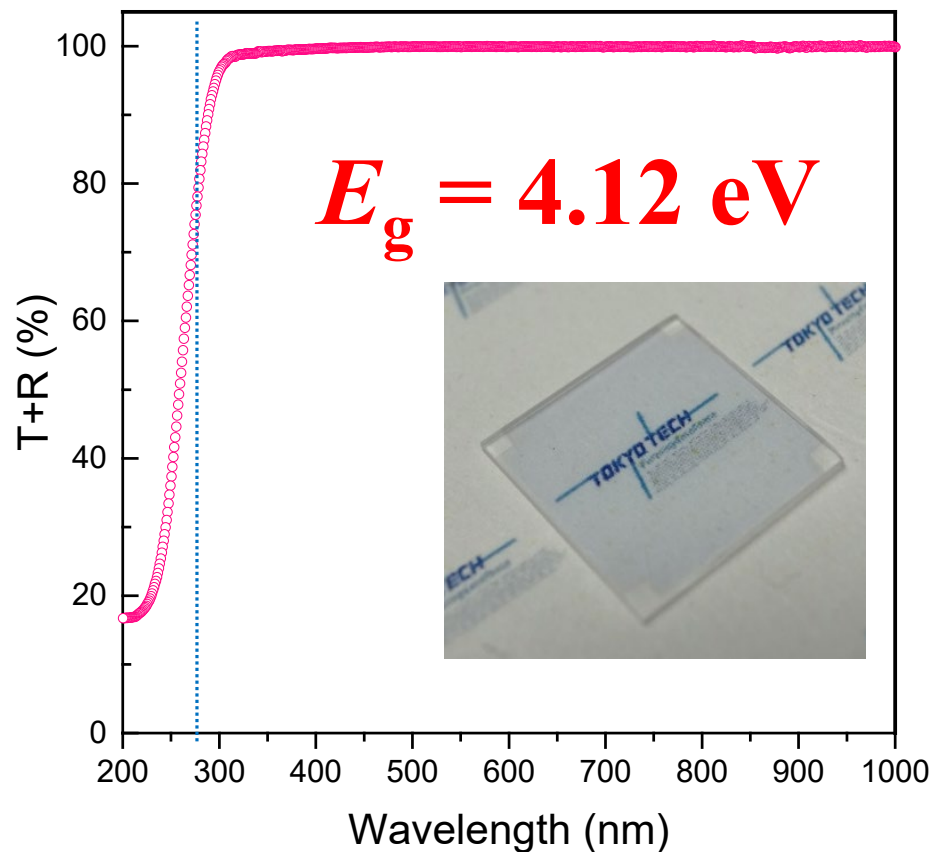
Reduce traps (voids and excess O)
Increase film density => Conducting a-Ga₂O₃

Best film (~5.4 g/cm³): N_e ~ 1×10^{14} cm⁻³, μ_{Hall} ~ 6 cm²/Vs

Better recipe for better stability

1. Good deposition chamber

Reduce impurity hydrogen and excess oxygen

Too high optimized P_{O2} would be a bad signature.

But, some hydrogen would be needed

2. Optimize deposition condition

$\sigma = 10^{-6} - 10^{-3}$ S/cm

$V_{th} \sim 0$ V

Smaller S, larger μ

Smaller subgap optical absorption, deep near-VBM defects

High-density film, Lower pressure, Higher (RF/AC/DC) power

3. Post-fabrication thermal annealing at 300 – 400ºC

Improve uniformity and stability

Too high temperature annealing would not be good

(hydrogen depletion / excess oxygen would deteriorate)

4. Not use H-containing process for over layers (ESL, passivation)

Typical deposition condition

Sputtering target	: 3"ϕ polycrystalline InGaZnO$_4$
Base pressure	: 10^{-4} Pa
Substrate–target distance (D)	: 55 mm
Total pressure (P)	: 0.55 Pa

 MFP = 12 mm, $N(D, P)$ = 4.4

Ar: O$_2$ ratio (R_{O2}) : 19.4: 0.6 sccm (R_{O2} = 2 − 3 %)

$\Gamma(300K) = 1.3\times10^{18}$ (Ar), 4.4×10^{16} (O$_2$) cm^{-2}s^{-1}

cf. # of O ions per surface area: 1.3×10^{15} cm^{-2} (d(a-InGaZnO$_4$) = 6.0 gcm^{-3})

Sticking probability of O: ~ 20% for growth rate of 0.5 Å/s

without sputtering energy and plasma potential

RF power : 70 W / 3" ϕ = 1.5 W/cm^2

Substrate temperature (T_s) : No intentional heating

(surface T raised to ~40°C for a-IGZO / ~140°C for Y$_2$O$_3$ [Yabuta et al., APL **89**, 112123 (2006)])

Mean free path (MFP): $\lambda = \dfrac{k_B T}{\sqrt{2}\sigma P} = \dfrac{K}{P[\text{Pa}]}$ [mm] (σ: Collision cross section)

Number of collision: $N(D, P) = D/\lambda = \dfrac{\sqrt{2}\sigma}{k_B T} \boxed{PD}$

	H$_2$	N$_2$	O$_2$	Ar	Kr
σ [nm^2]	0.231	0.430	0.396	0.402	0.523
K at 300K	12.7	6.81	7.40	7.29	5.60

Surface bombardment flux:

$\Gamma = \dfrac{n v_a}{4} = n\sqrt{\dfrac{k_B T}{2\pi M}} = \dfrac{P}{\sqrt{2\pi M k_B T}} = K_\Gamma \dfrac{P[\text{Pa}]}{\sqrt{M}}$ [(cm^{2}s)$^{-1}$] $K_\Gamma(300K) = 1.5\times10^{19}$

CONTENT for AOS TFT

Doping in crystalline oxides

Substitution: Larger ion charge: Electron doping

$$Zn^{2+}O + Ga => Zn^{2+}O:Ga^{3+} + e^- + Zn$$

$$Zn_{Zn} + Ga(s) => Ga_{Zn}^{\cdot} + e^- + Zn(s)$$

Oxygen deficiency (Extra cation): Electron doping

$$Zn^{2+}O => Zn^{2+}O:V_O^{2+} + 2e^- + 1/2O_2$$

Cation deficiency (Extra oxygen): Hole doping

$$Zn^{2+}O => Zn^{2+}O:V_{Zn}^{2-} + 2h^+ + Zn(s)$$

Hydrogen: Electron doping

$$Zn^{2+}O + 1/2H_2 => Zn^{2+}O:H_i^+ + e^-$$
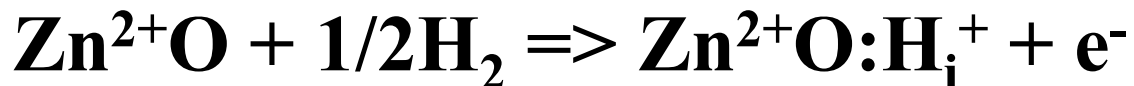
No substitution doping in amorphous oxide

- Substitution of Zn^{2+} with Ga^{3+} in c-ZnO…
  generates a free electron

- Atomic site is not definable in amorphous
  a-Si is exception: Si takes a rigid tetrahedral site

- Substitution of Zn^{2+} with Ga^{3+} in a-IGZO…
  Compensated by excess $1/2 O^{2-}$
  during deposition/annealing

Doping in amorphous oxides
- Off stoichiometry of oxygen ion
- Addition of hydrogen

Ion charge stoichiometry (charge neutrality) is important for AOS

Charge neutrality: Determine doping
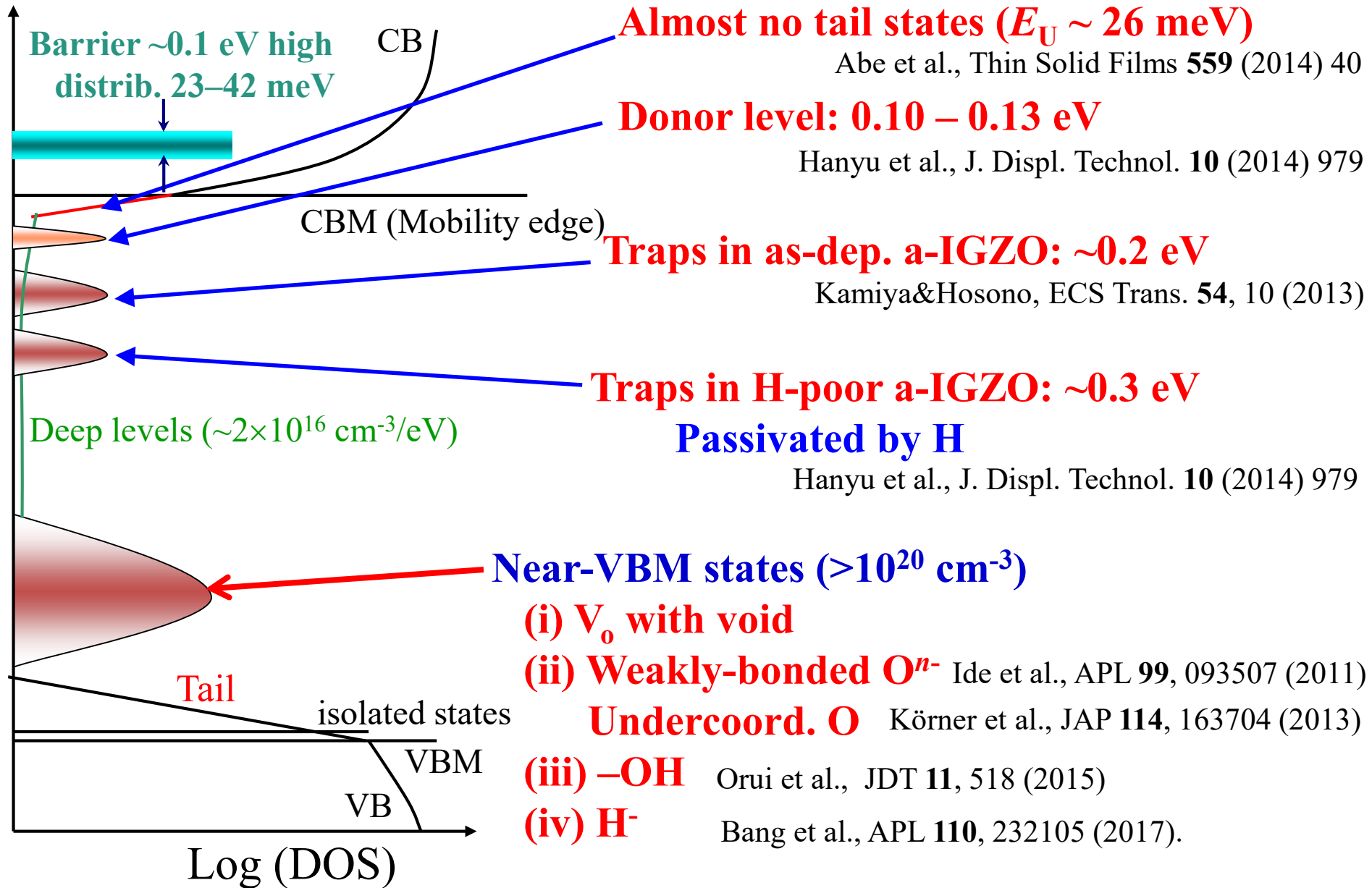Oxygen deficiency: Donor & Trap
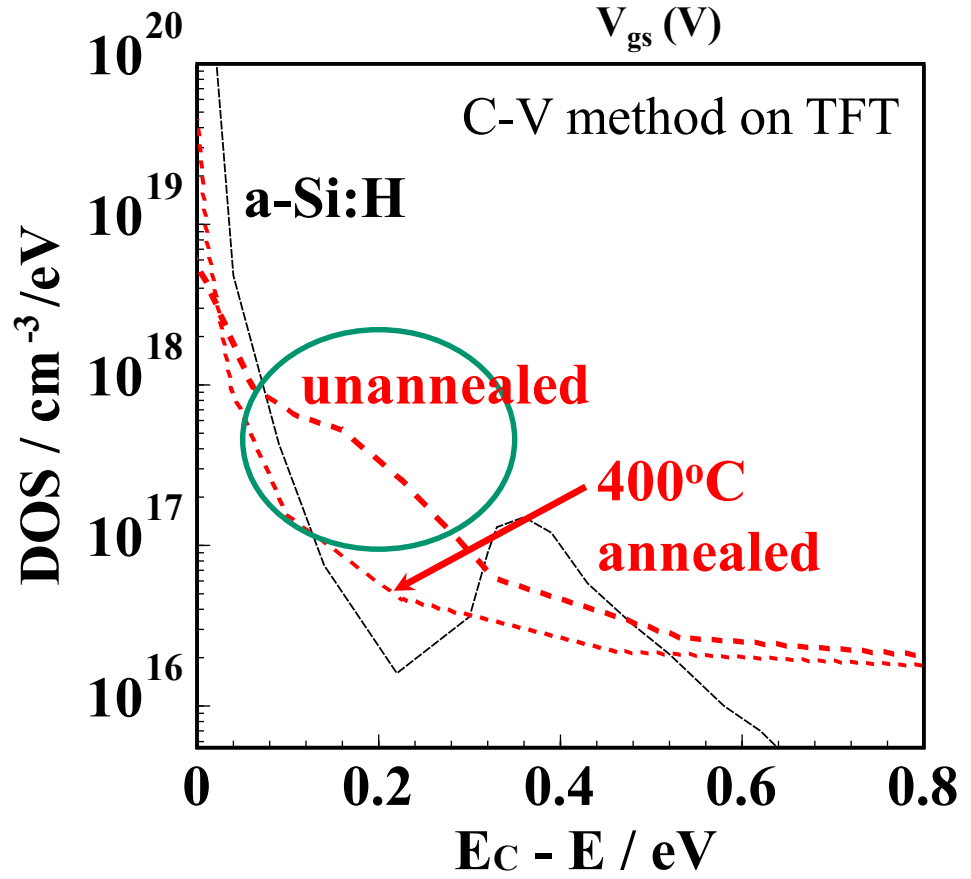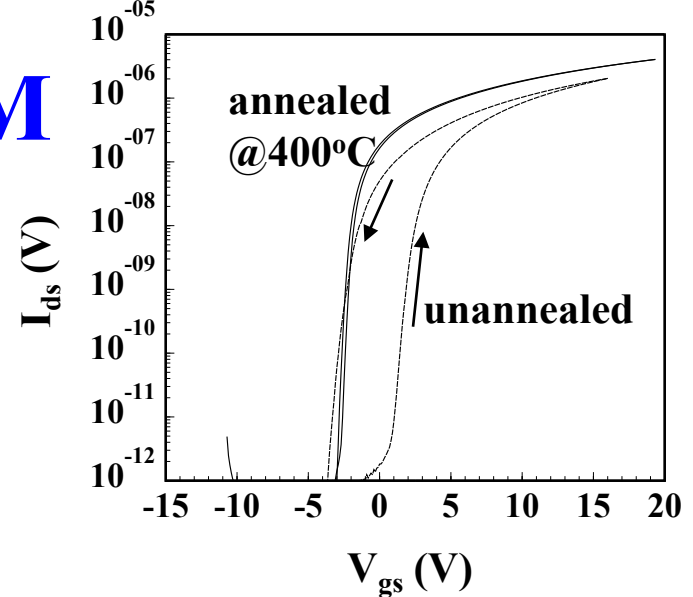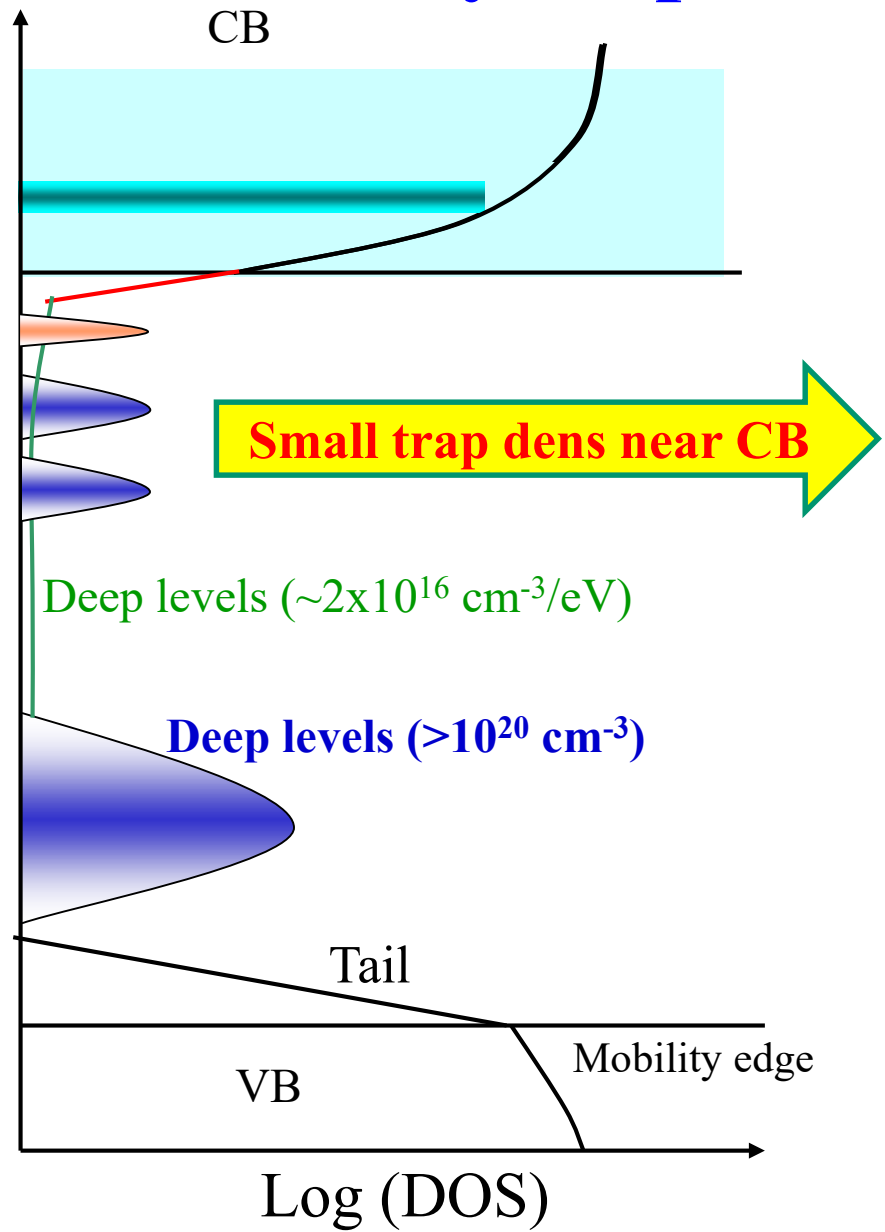Excess oxygen?
Hydrogen?

CONTENT for AOS TFT

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5. Doping
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7. Why too large P_{O2} is bad?:
   Weakly-bonded Oxygen
8. Annealing
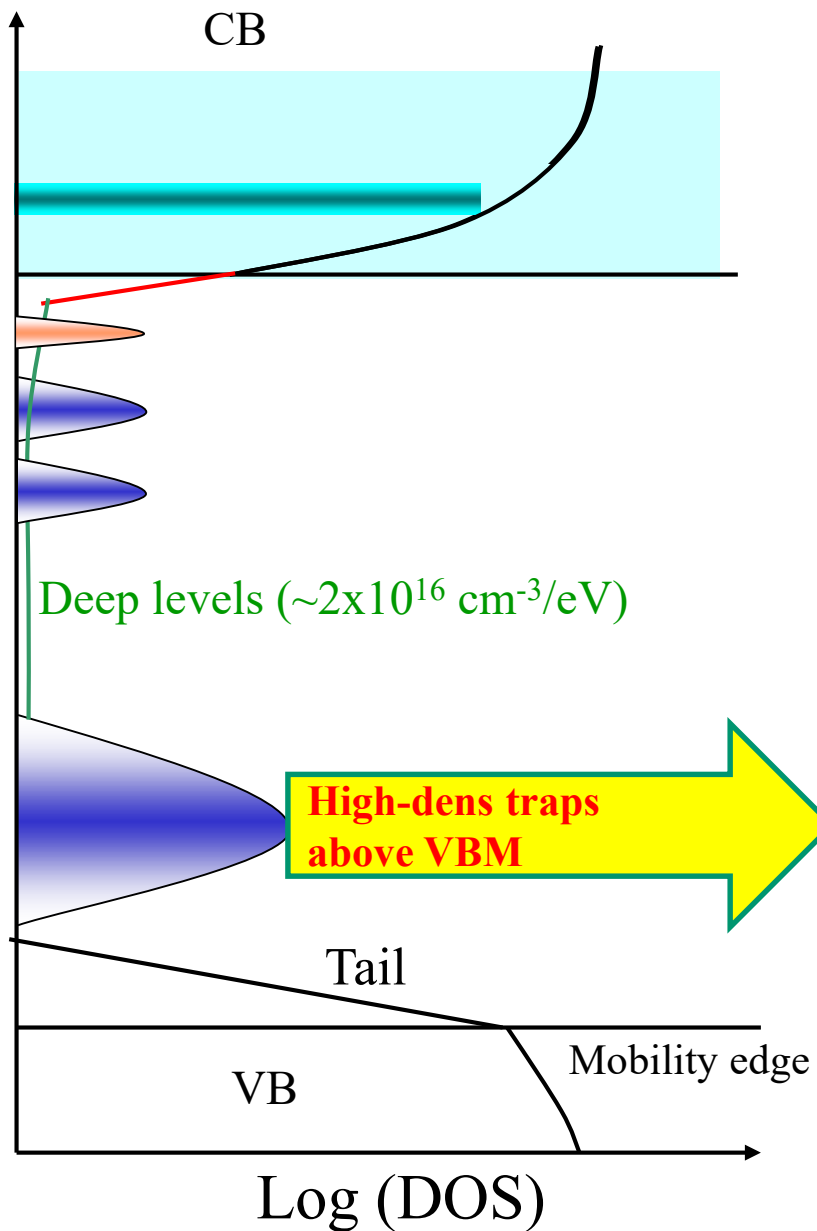9. Hydrogen

Electronic structure of a-IGZO

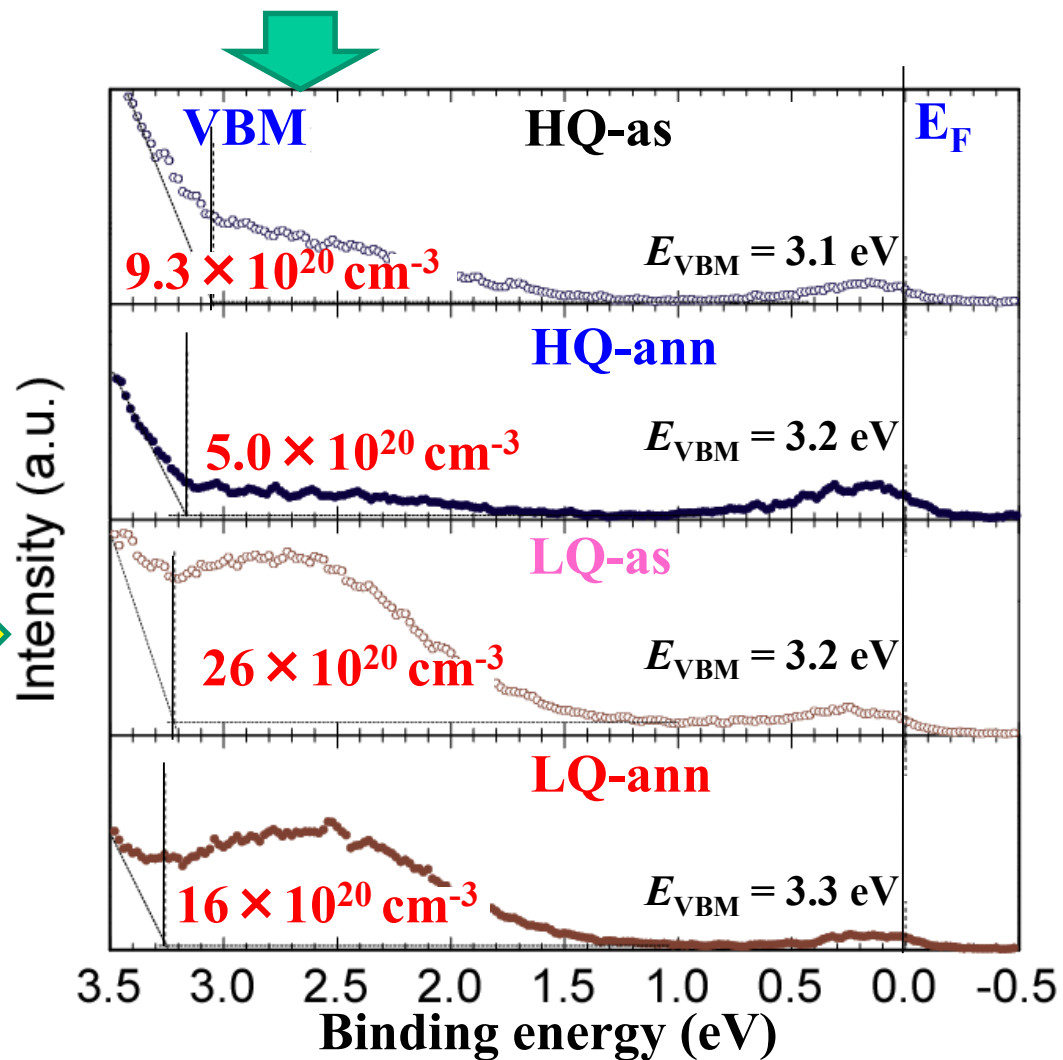Barrier ~0.1 eV high distrib. 23–42 meV

CB

CBM (Mobility edge)

Deep levels ($\sim 2\times10^{16}$ cm^{-3}/eV)

Tail

isolated states

VBM

VB

Log (DOS)

Almost no tail states ($E_U \sim 26$ meV)

Abe et al., Thin Solid Films **559** (2014) 40

Donor level: 0.10 – 0.13 eV

Hanyu et al., J. Displ. Technol. **10** (2014) 979

Traps in as-dep. a-IGZO: ~0.2 eV

Kamiya&Hosono, ECS Trans. **54**, 10 (2013)

Traps in H-poor a-IGZO: ~0.3 eV

Passivated by H

Hanyu et al., J. Displ. Technol. **10** (2014) 979

Near-VBM states (>10^{20} cm^{-3})

(i) V_o with void

(ii) Weakly-bonded O^{n-} Ide et al., APL **99**, 093507 (2011)

Undercoord. O Körner et al., JAP **114**, 163704 (2013)

(iii) –OH Orui et al., JDT **11**, 518 (2015)

(iv) H$^-$ Bang et al., APL **110**, 232105 (2017).

Low-density traps near CBM

CB

Small trap dens near CB

Deep levels (~2x10^{16} cm^{-3}/eV)

Deep levels (>10^{20} cm^{-3})

Tail

VB

Mobility edge

Log (DOS)

annealed @400°C

unannealed

I_{ds} (V)

V_{gs} (V)

C-V method on TFT

a-Si:H

unannealed

400°C annealed

DOS / cm^{-3}/eV

E_C - E / eV

High-density near-VBM states: by HAXPES

PLD, HAXPES: 8 keV

Subgap absorption/photoresonse

Barrier ~0.1 eV high distrib. 23–42 meV

CB

CBM

Donor level: 0.10 – 0.13 eV
Traps in as-dep. a-IGZO: ~0.2 eV
Traps in H-poor a-IGZO: ~0.3 eV

Deep levels (~2×10^{16} cm^{-3}/eV)

Subgap absorption Photoresponse > 2.3 eV

~1.5 eV

Near-VBM states (>10^{20} cm^{-3})

Tail

isolated states

VBM

VB   VB

Log (DOS)

unannaled

LQ

annealed

HQ

α (cm^{-1})

10^5

10^4

10^3

Photon energy / eV

1.0   2.0   3.0   4.0   5.0

Unanneled (closed symbols)
σ_D (Scm^{-1}) = 2x10^{-5}~ 5x10^{-3}

σ_{ph} (Scm^{-1})

10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}

—O— SC-IGZO
σ_D (Scm^{-1}) = 2x10^{-5}

Photon energy (eV)

1.5   2.0   2.5   3.0   3.5   4.0
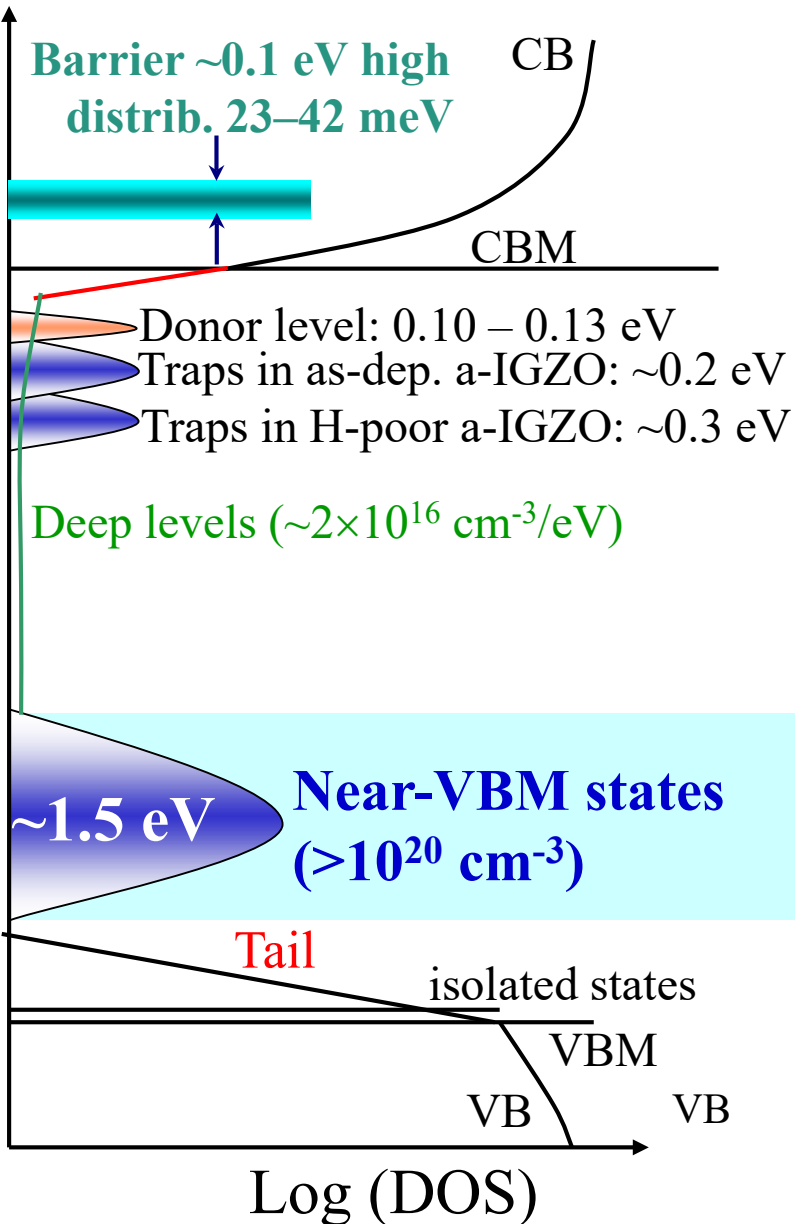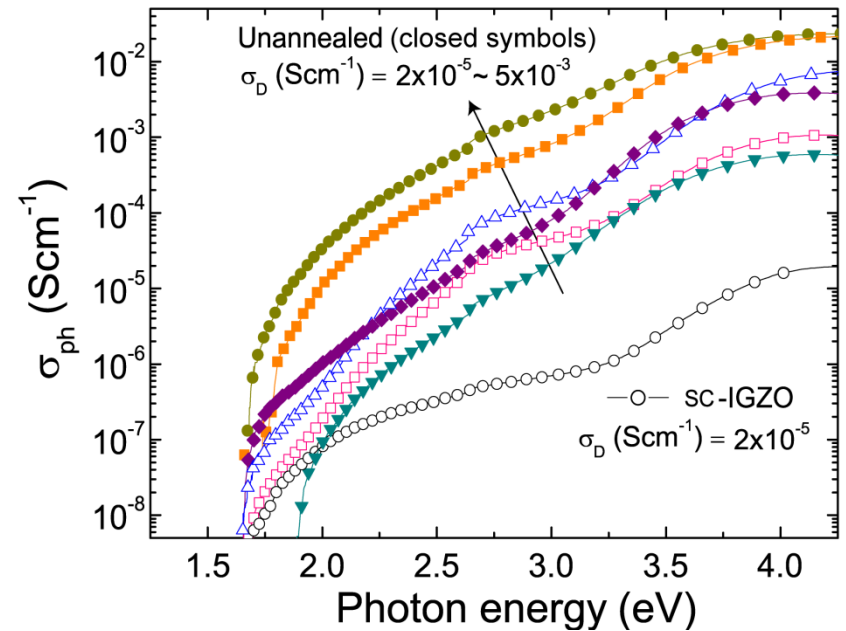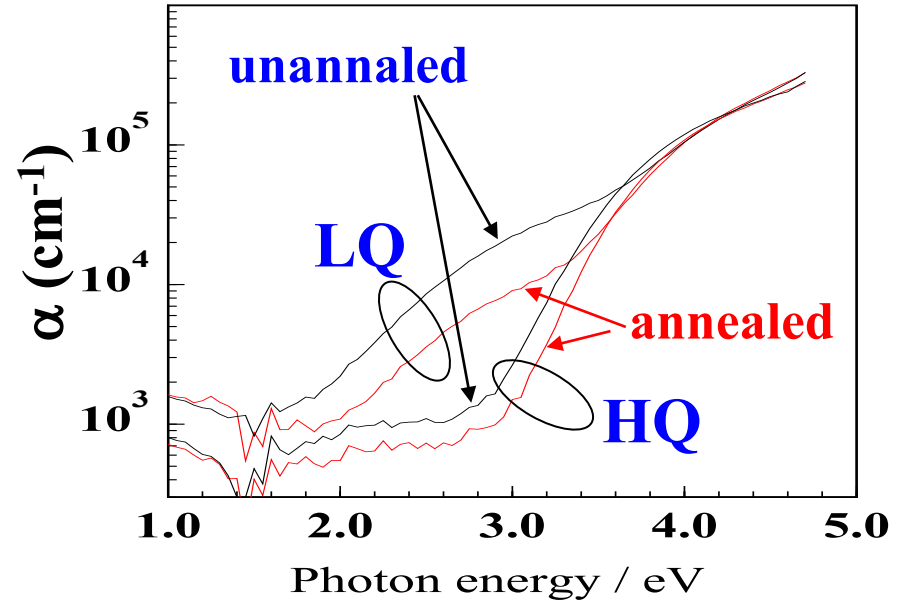
Why off current is so low?

- **Wide gap of a-InGaZnO$_4$ (~3.2 eV)**
  No limitation for inversion operation
- **Low hole mobility**
  $\mu_h \sim 0.01$ cm^2/Vs still larger than that of a-Si:H
- **Schottky contact for valence band**
  One possibility
  Would not be able to explain the constant off current

=> Fermi level pinning deep in band gap
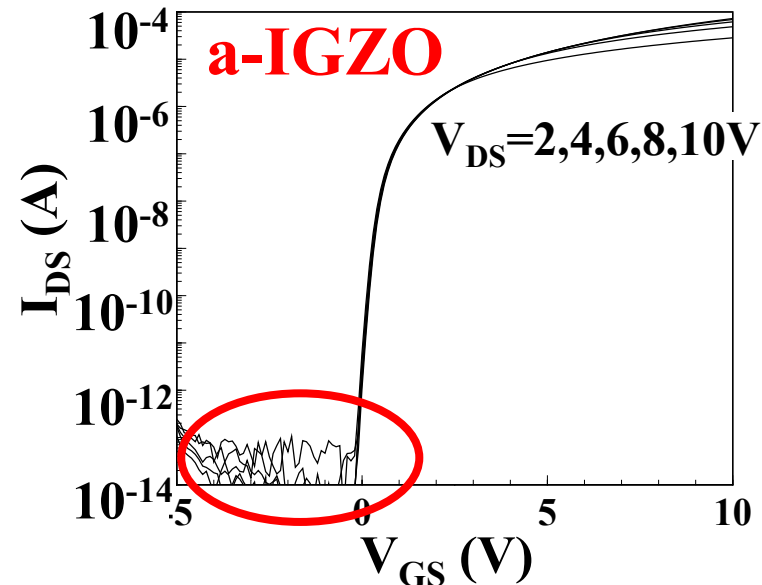
Origin of low off current

J. Jeong, Y. Hong, *Debye Length and Active Layer Thickness-Dependent Performance Variations of Amorphous Oxide-Based TFTs,* IEEE Trans. Electron Devices **59** (2012) 710

Abstract—We analyzed the active layer thickness-dependent performance variations of amorphous oxide-based semiconductor thin-film transistors (AOS TFTs), which are typically operated in depletion mode by using an ATLAS 2-D device simulator. The negative shift of threshold voltage was originated from increasing the amount of intrinsic carrier as active layer thickness is increased. On the contrary, OFF-current level was a function of Debye length, which is in inverse proportion to the square root of carrier density and the amount of valence band deep states, as well as active layer thickness. Therefore, the relation between Debye length and active layer thickness determines the OFF-current level, which also enables to explain the OFF-current behavior of AOS TFTs under light illumination.

Parameter	Value	Unit
W_{TA}	0.18	eV
N_{TA}	3.5×10^{17}	$cm^{-3} eV^{-1}$
W_{GA}	0.21	eV
N_{GA}	1.6×10^{16}	$cm^{-3} eV^{-1}$
$E_C - E_{GA}$	1.34	eV
W_{TD}	not considered	eV
N_{TD}	not considered	$cm^{-3} eV^{-1}$
W_{GD}	variable	eV
N_{GD}	variable	$cm^{-3} eV^{-1}$
$E_C - E_{GD}$	2.4	eV
μ_{n0}	12	$cm^2 V^{-1} s^{-1}$
μ_{p0}	not considered	$cm^2 V^{-1} s^{-1}$
E_G	3.2	eV
N_C	5×10^{18}	cm^{-3}
N_V	not considered	cm^{-3}
ε_{AOS}	10	-
ε_{INS}	7.5	-
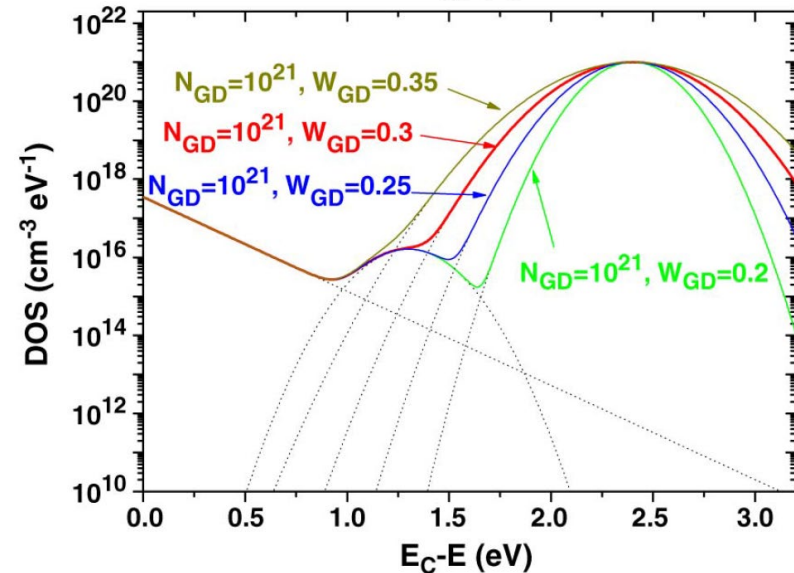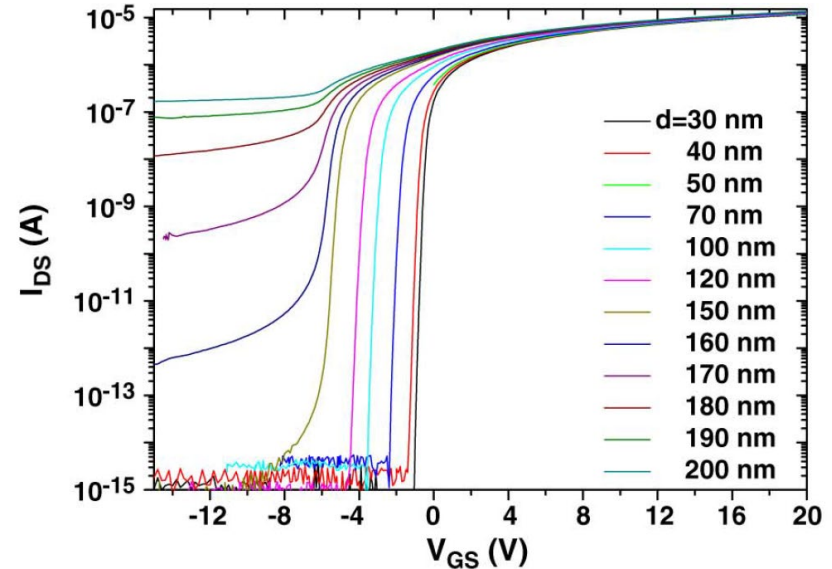
a-IGZO deposited by PLD in vacuum

By PLD
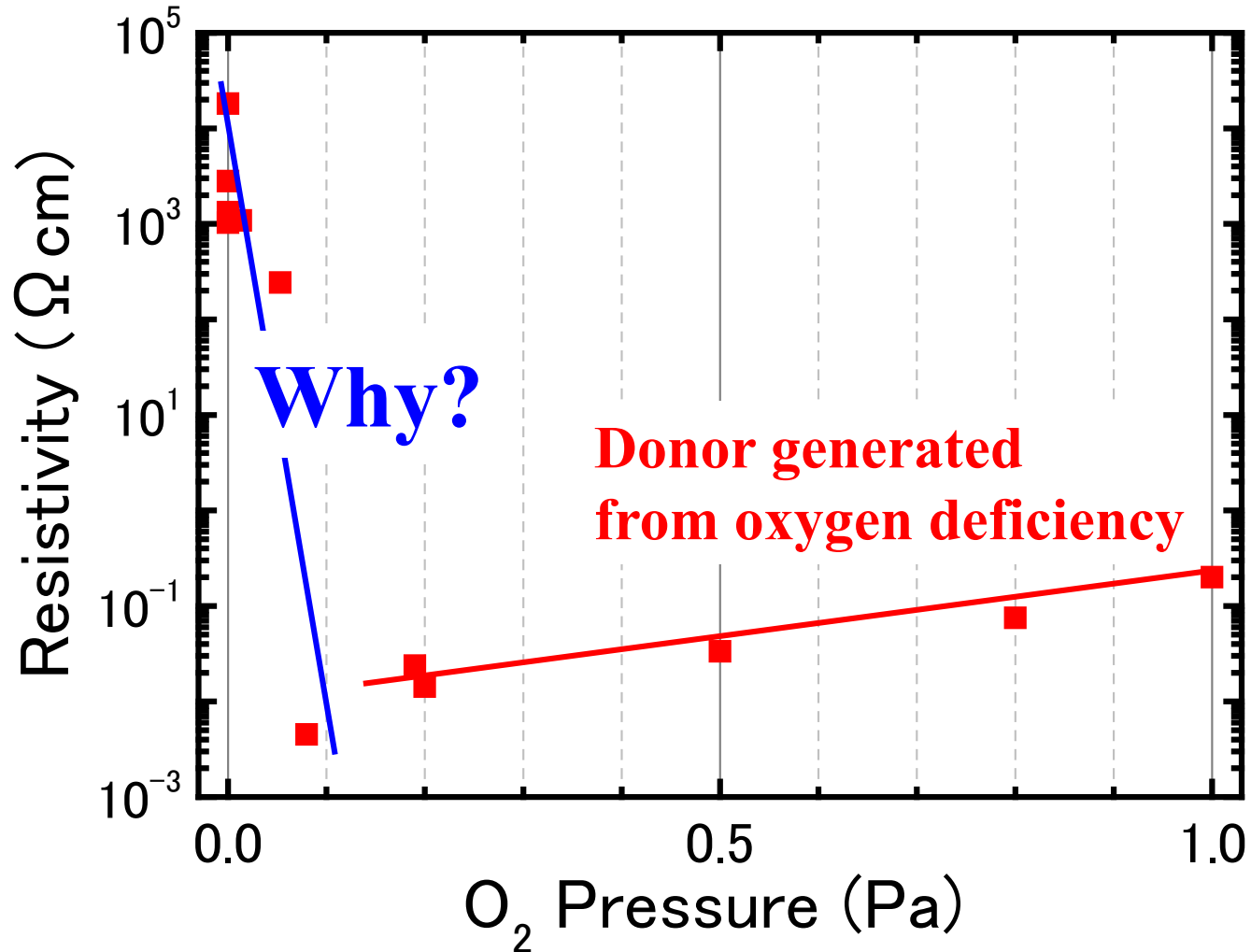
What happens in vacuum PLD-deposited a-IGZO?

By PLD
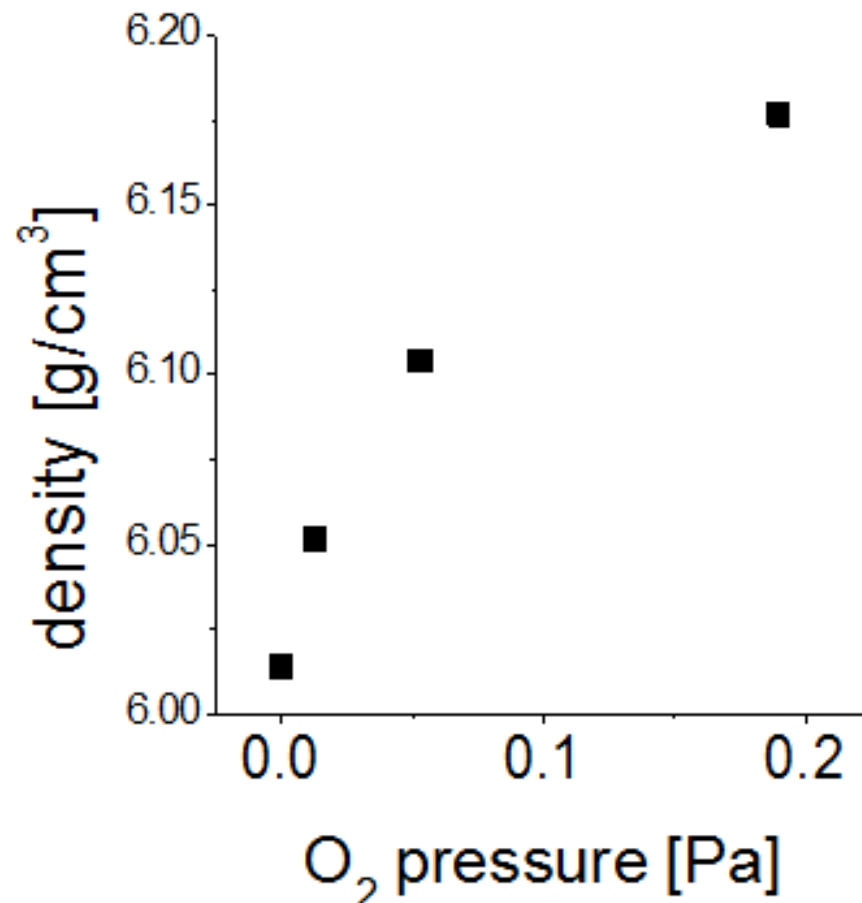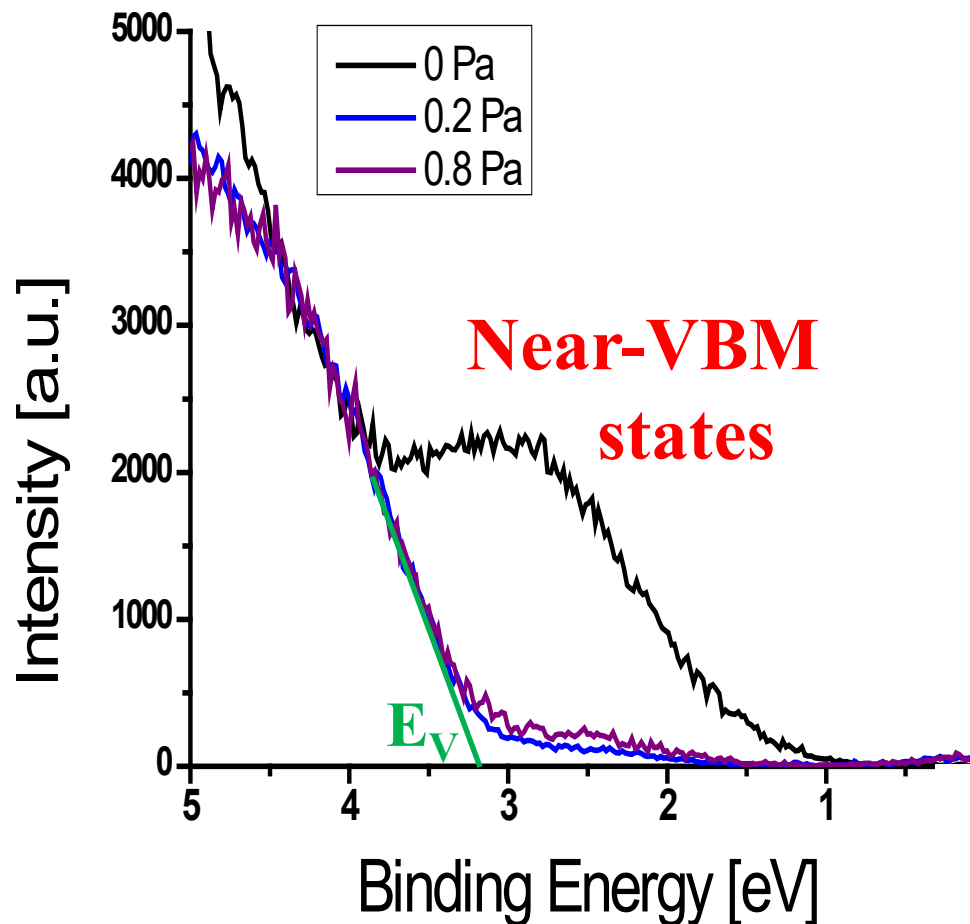
Charge compensation model
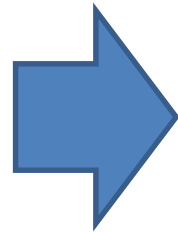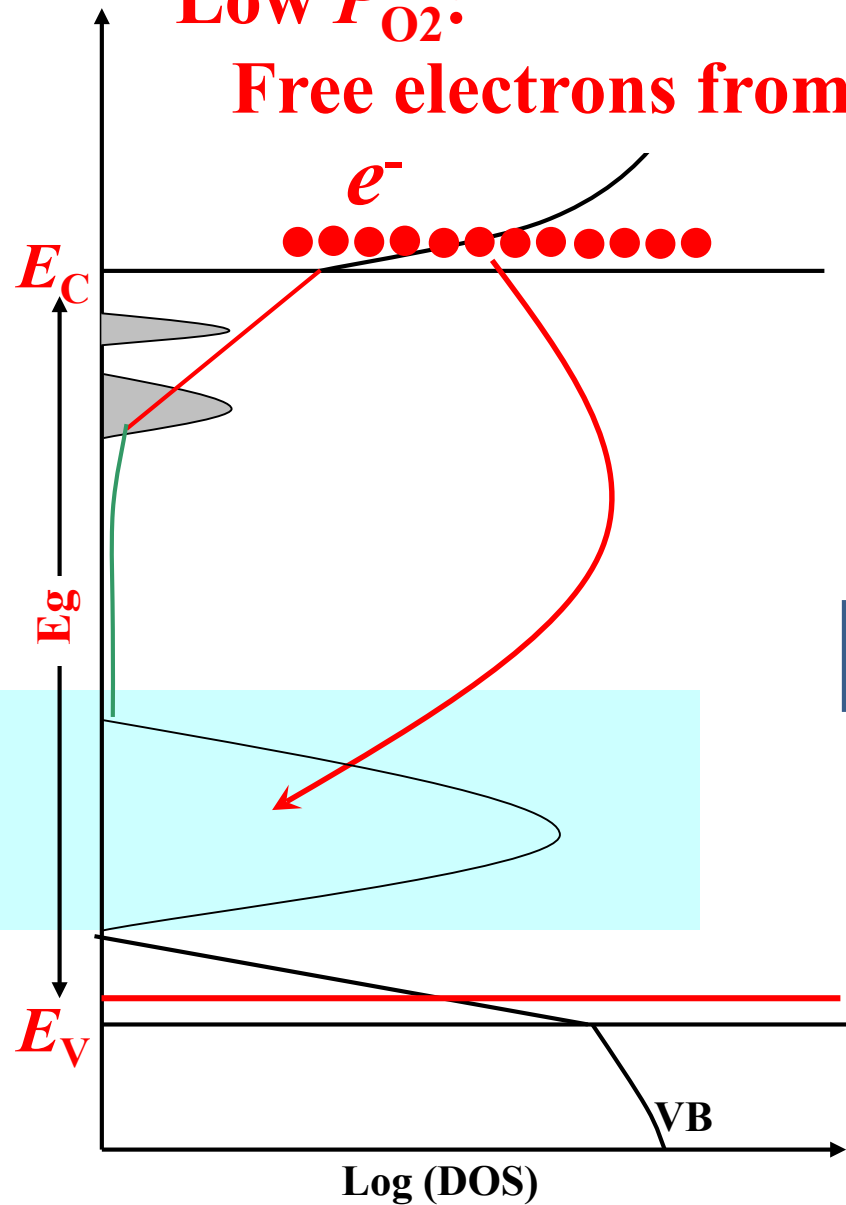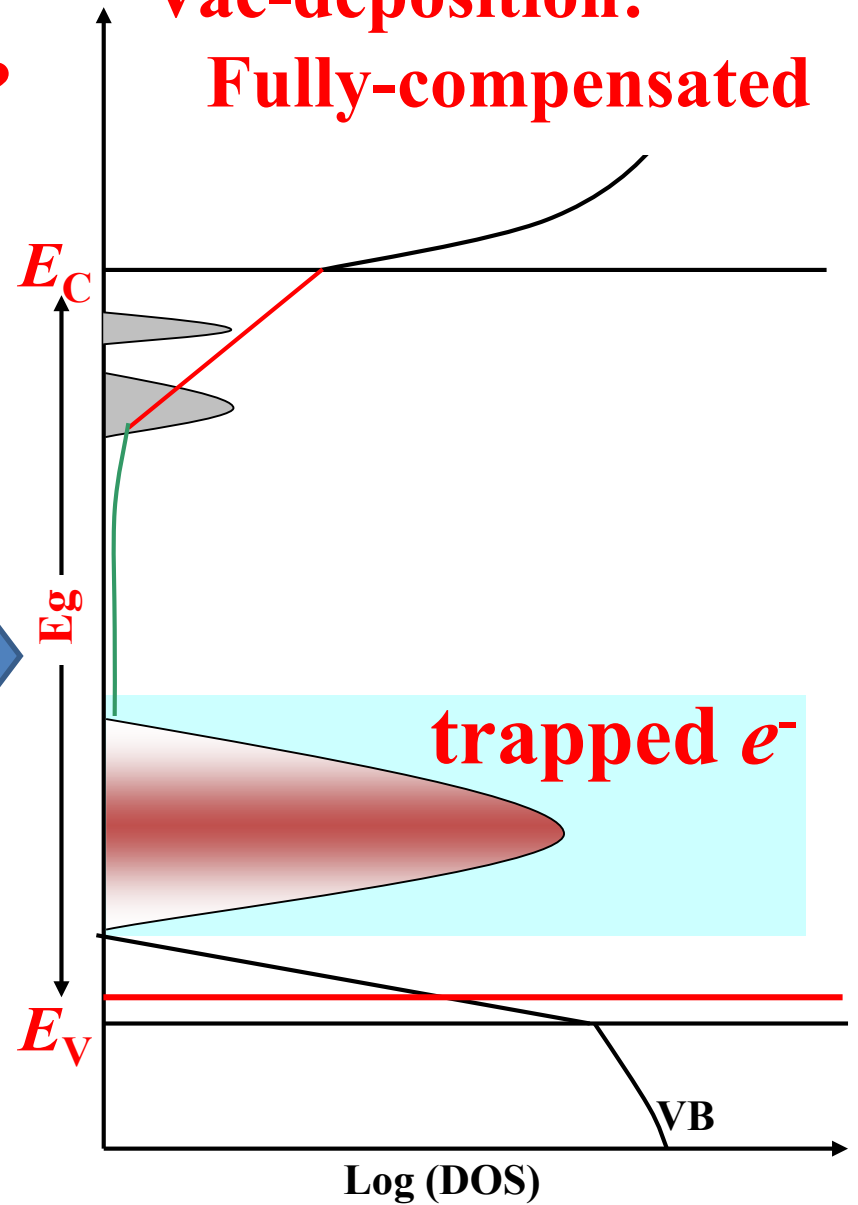
CONTENT for AOS TFT

1. Characteristics of a-IGZO TFT
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4. Growth condition and TFT fabrication
5. Doping
6. Defect structures (subgap defects)
7. **Why too large P_{O_2} is bad?:**
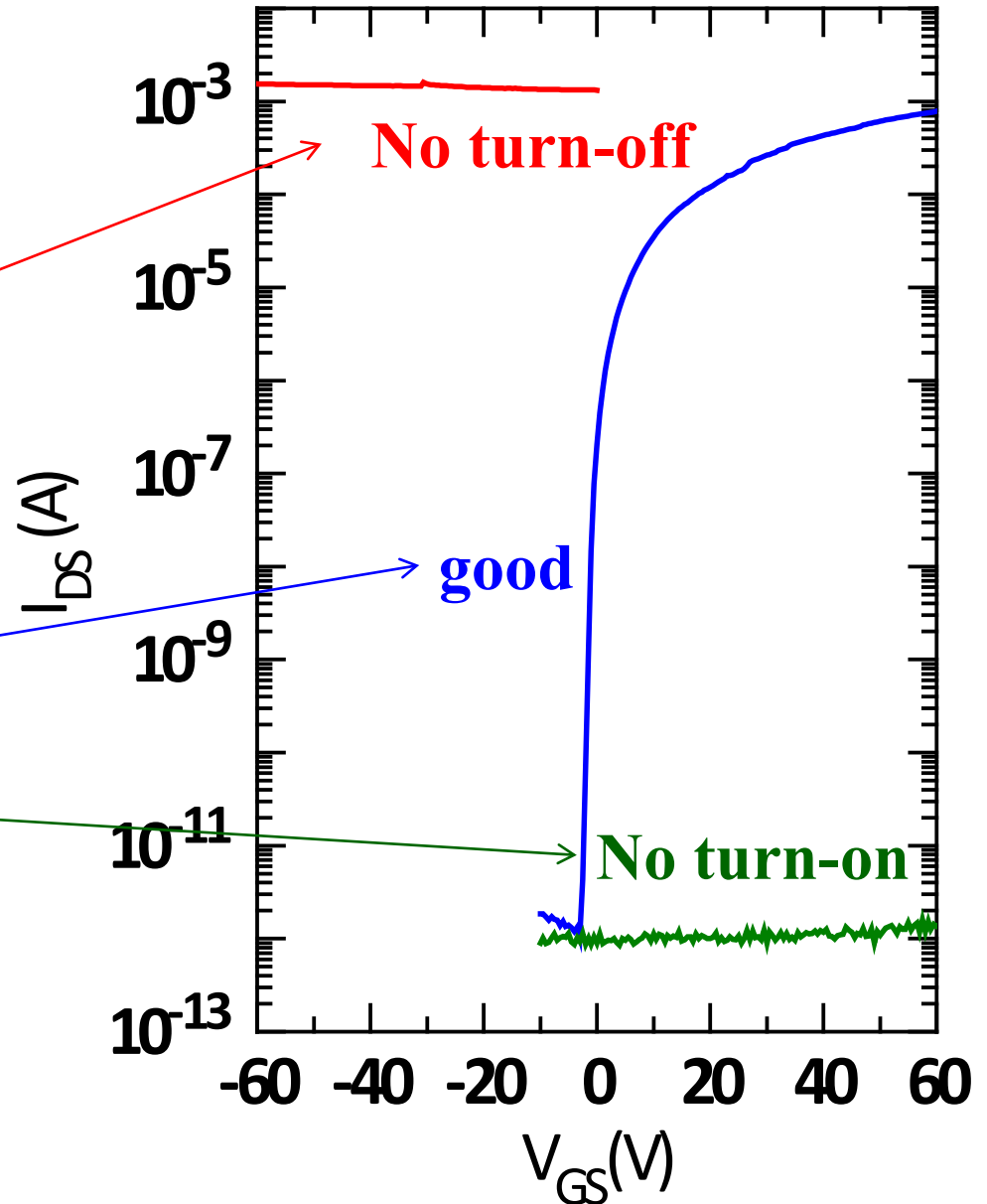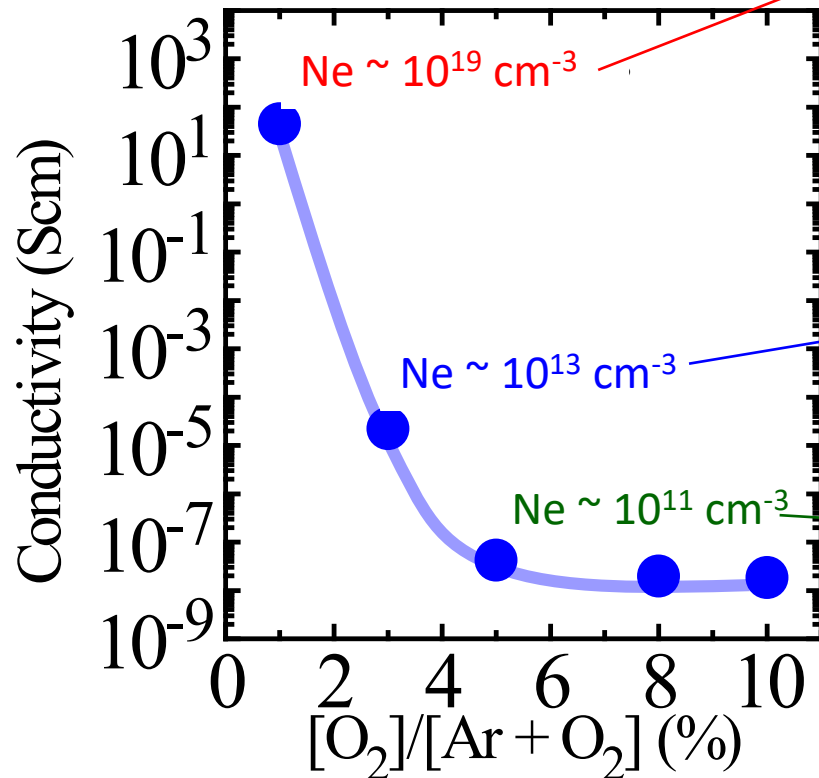   **Weakly-bonded Oxygen**
8. Annealing
9. Hydrogen

Optimum oxygen pressure

Good TFTs:

$N_D = 10^{12} - 10^{15}$ cm^{-3}

$\sigma = 10^{-6} - 10^{-3}$ Scm^{-1}

Ne ~ 10^{19} cm^{-3}

Ne ~ 10^{13} cm^{-3}

Ne ~ 10^{11} cm^{-3}

No turn-off

good

No turn-on

Conductivity (Scm)

[O$_2$]/[Ar + O$_2$] (%)

I_{DS} (A)

V_{GS}(V)

TFT characteristics (ozone annealing)
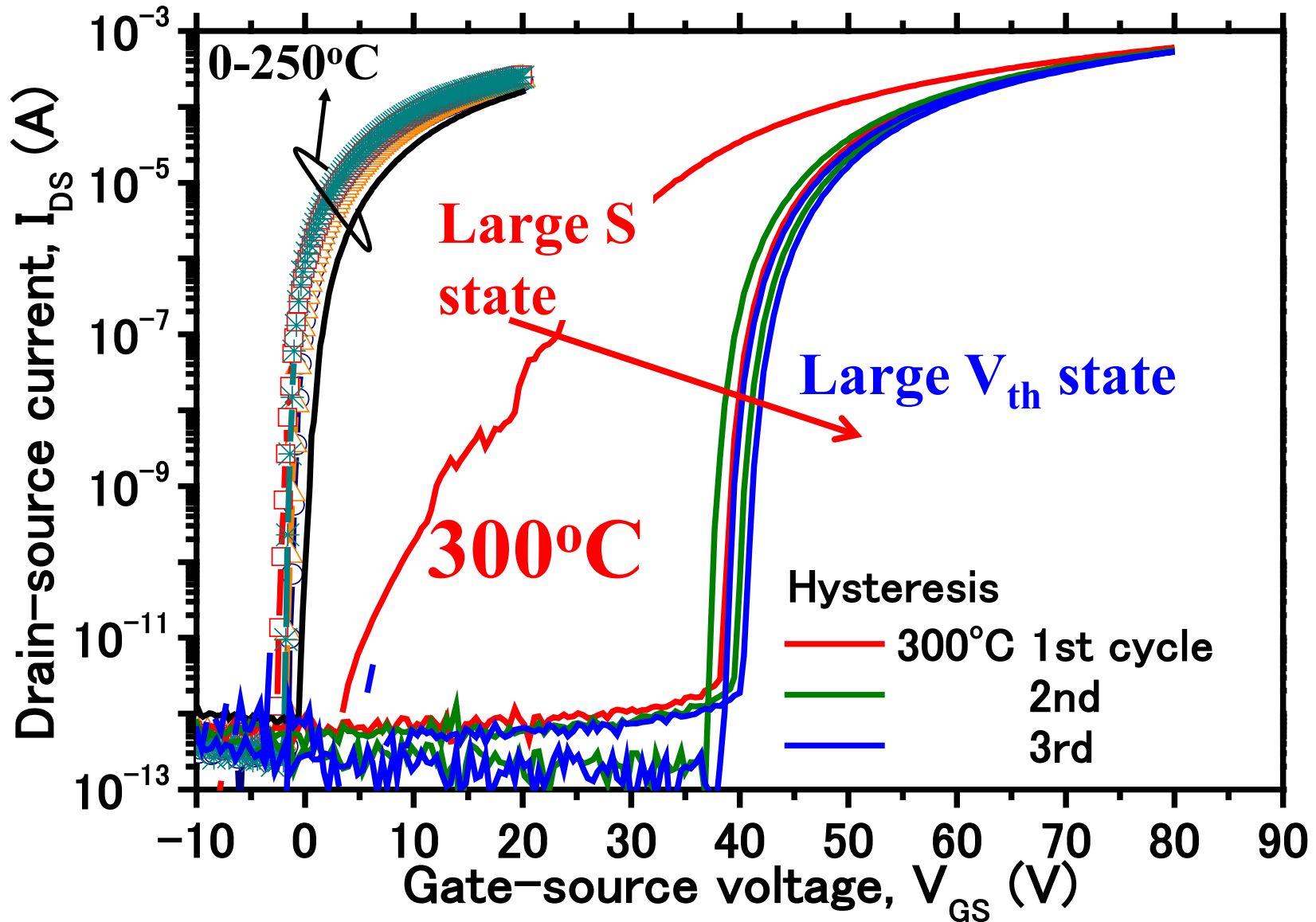
Recovery by monochromated photons
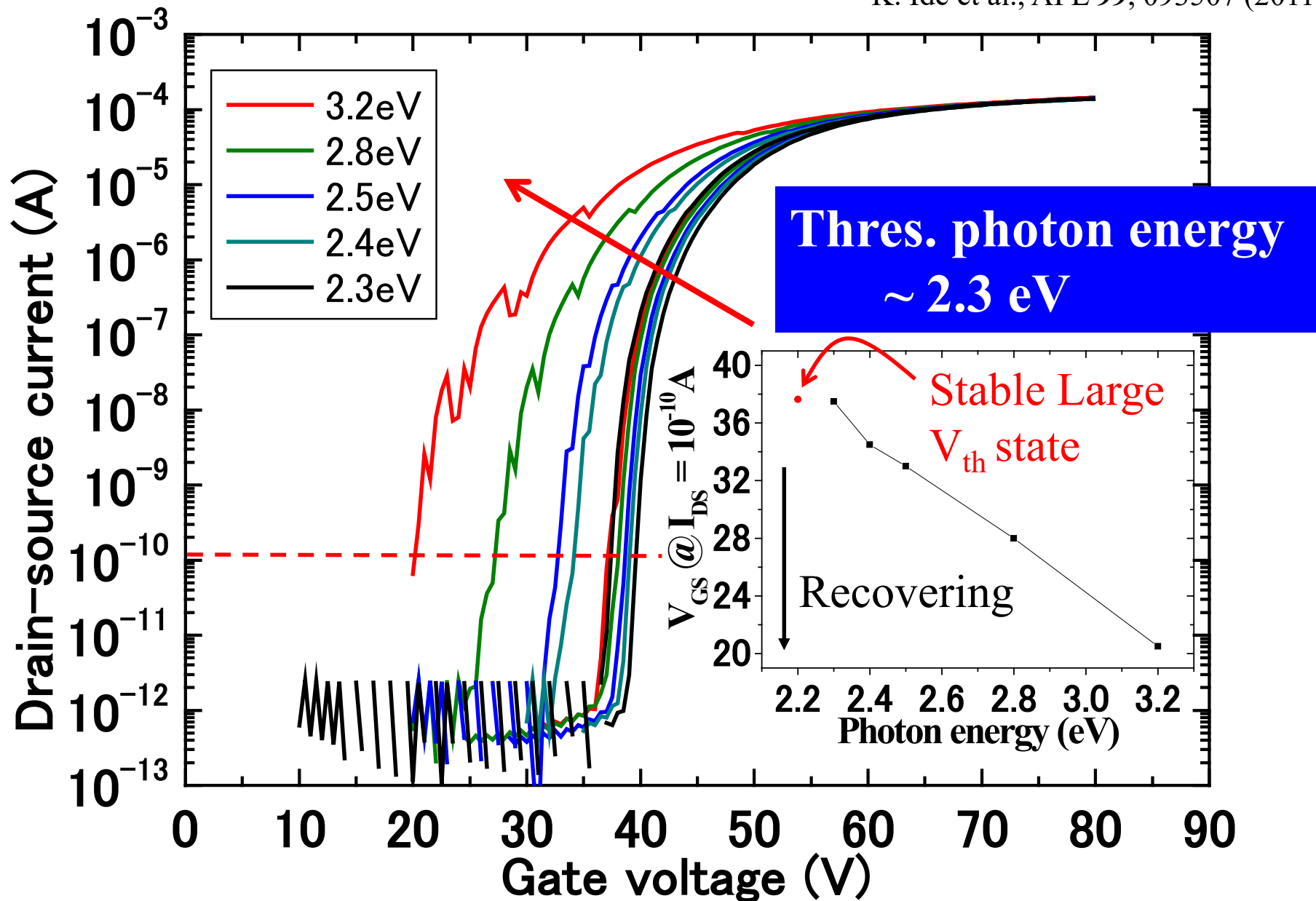
Thermal desorption spectra (TDS)
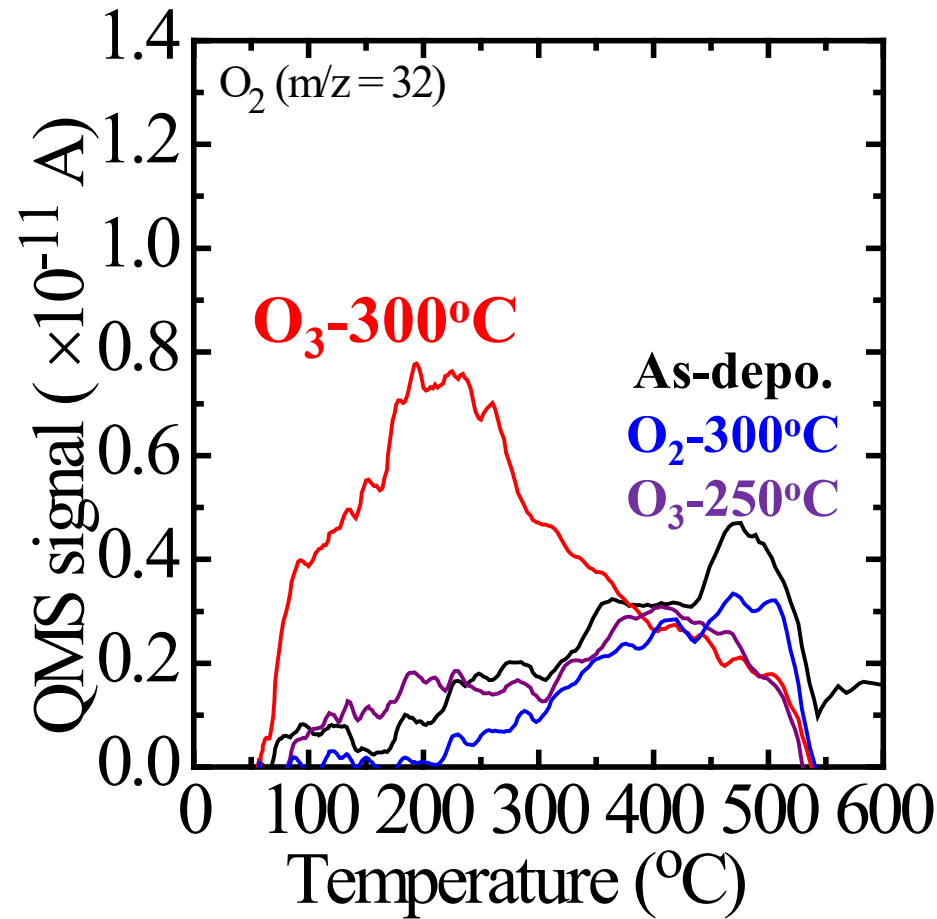
Weakly-bonded oxygen in SnO₂
N. Yamazoe et al., Surf. Sci. (1979)
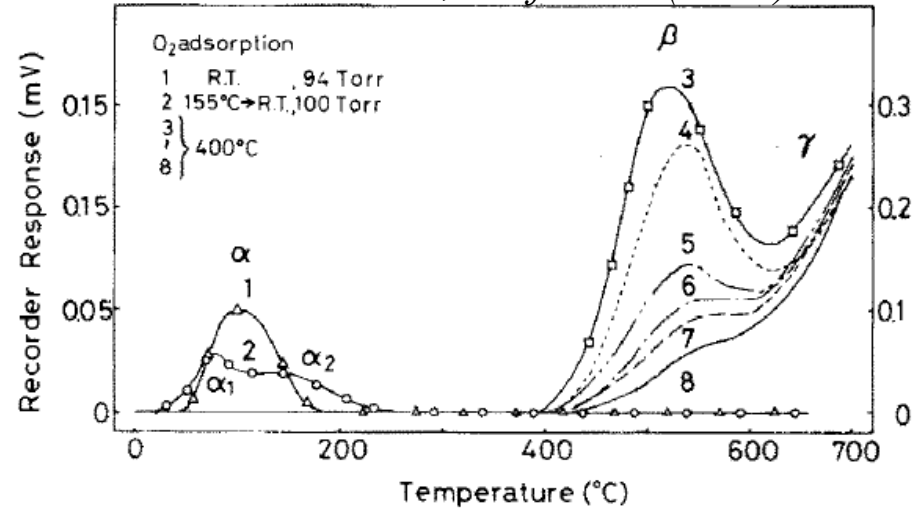
a-type (Low-temp.) : neutral O_2 or O_2^-
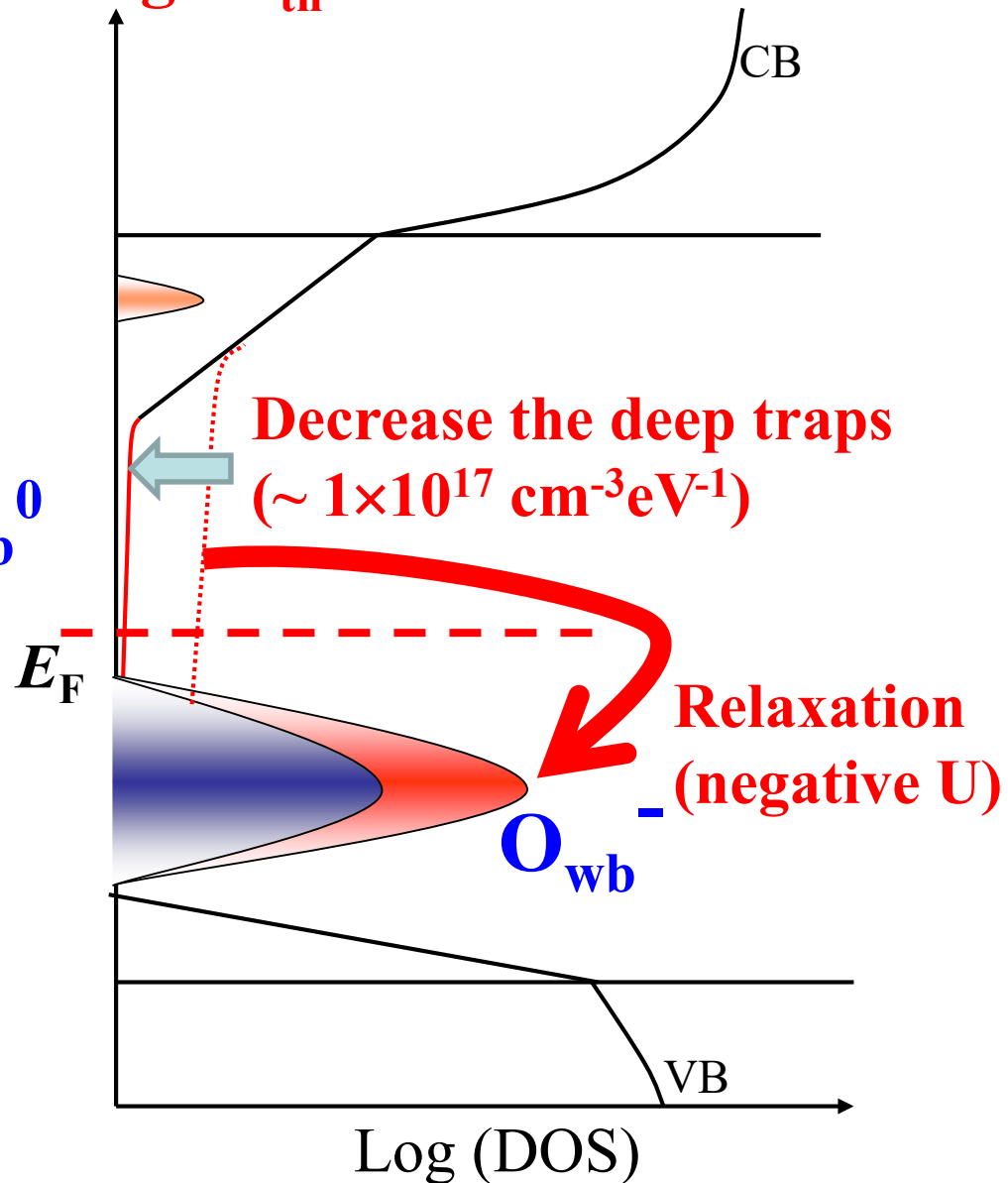b-type (High-temp.) : O^{2-} (lattice)

- **Large amount of O_2 desorption in 300°C O_3 annealed a-IGZO**
- **Weakly-bonded oxygen causes the bistable behavior on TFT operation**
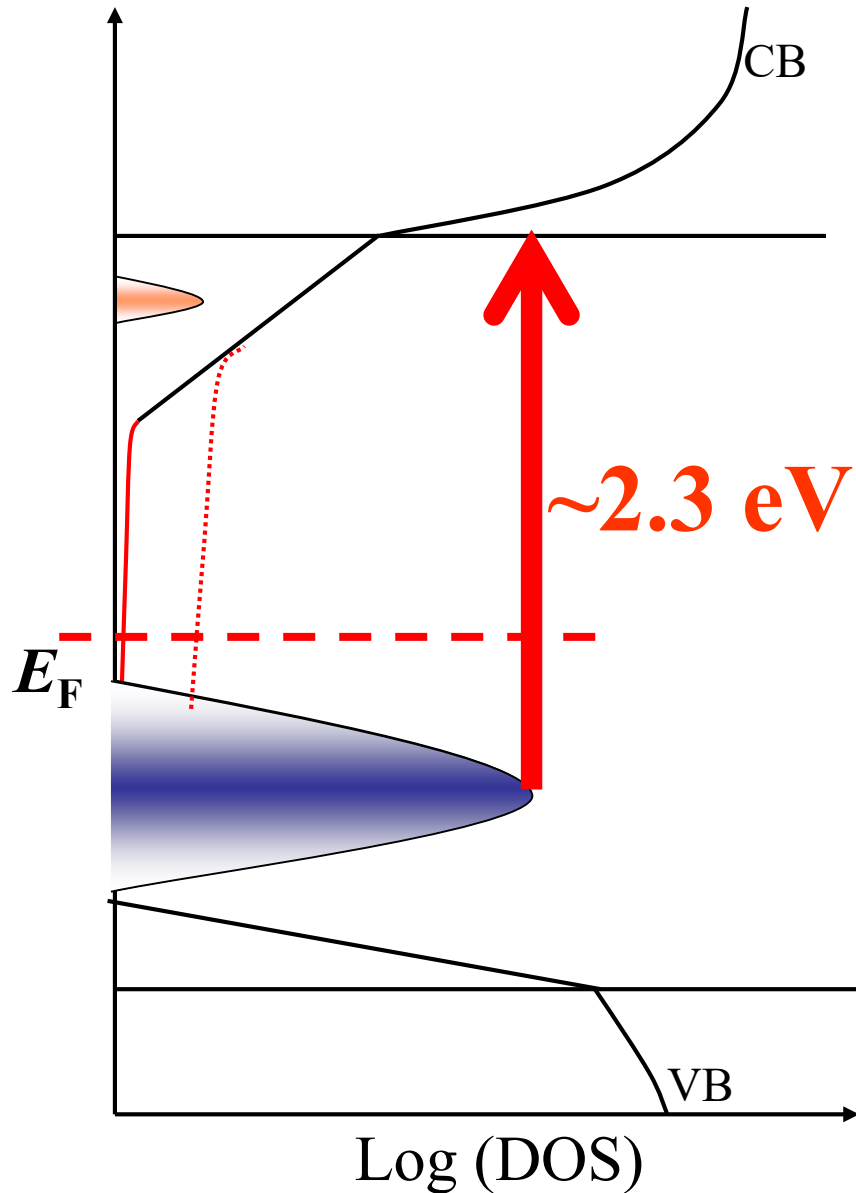
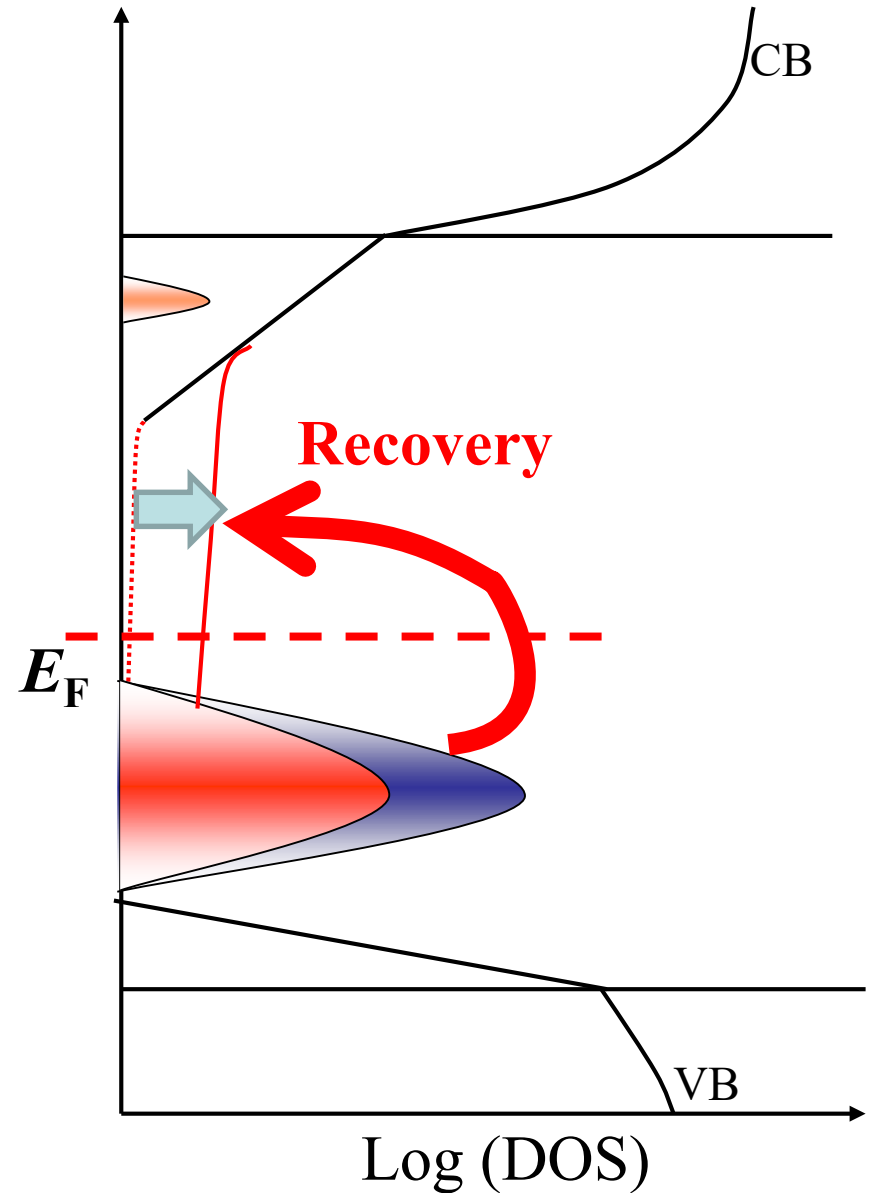# Model: Negative-U bistable states

Large S state

Large V$_{th}$ state

CB

Donor level ~0.1 eV

Deep continuous traps
(~ 4×10^{17} cm^{-3}eV^{-1})

O$_{wb}^0$

E_F

Deep levels (>> 10^{20} cm^{-3})
Surface states

CB

Decrease the deep traps
(~ 1×10^{17} cm^{-3}eV^{-1})

Relaxation
(negative U)

E_F

O$_{wb}^-$

VB

VB

Log (DOS)

Log (DOS)
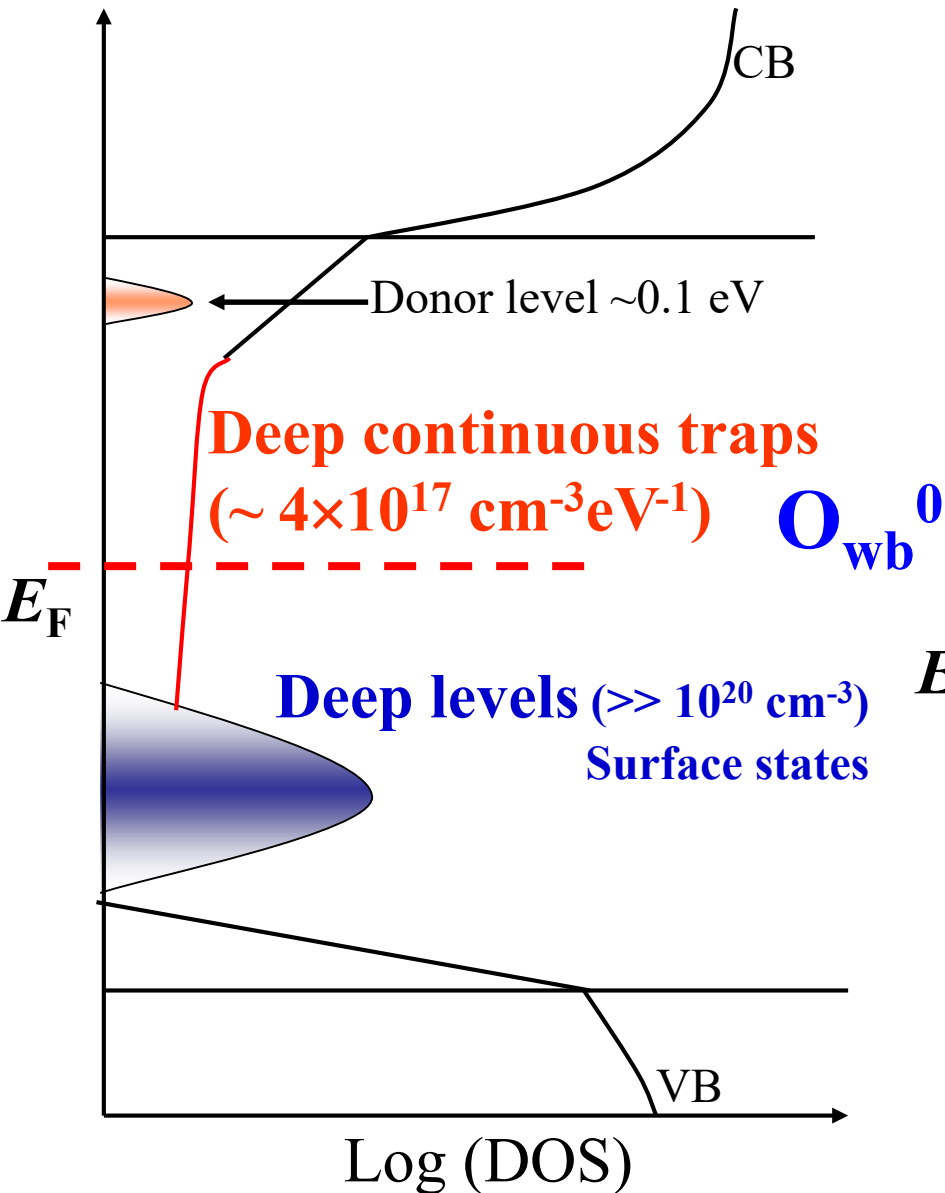
Recovery by light: Weakly-bonded oxygen

Photoexcitation

Recovery to Large S state

~2.3 eV

Recovery

E_F

CB

VB

Log (DOS)

a-IGZO TFT by very high P_{O2} sputtering

Sputtered at R_{O2} = 3-10%
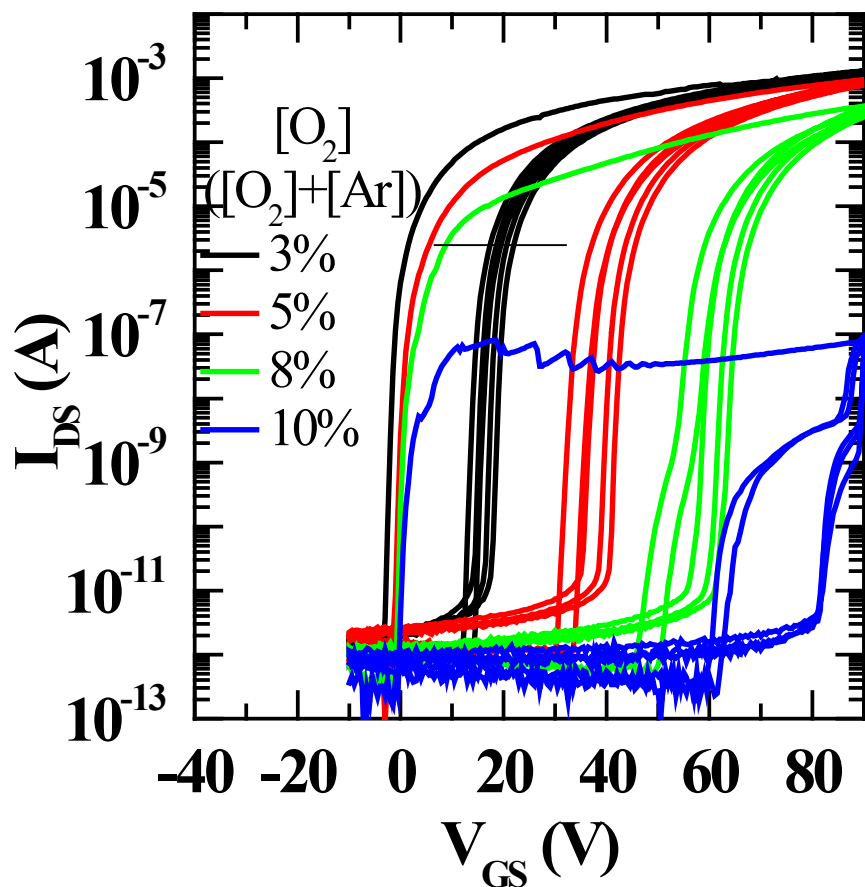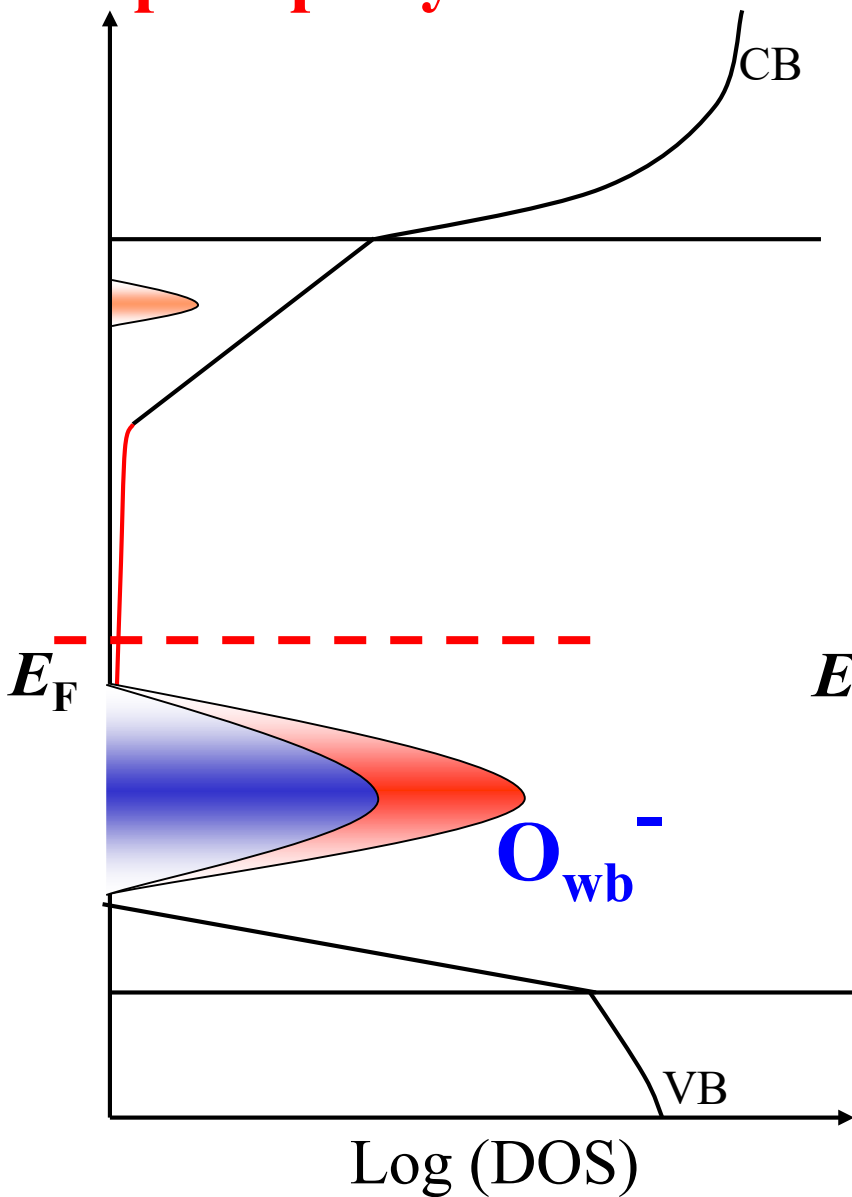
Sputtered at R_{O2} = 8%
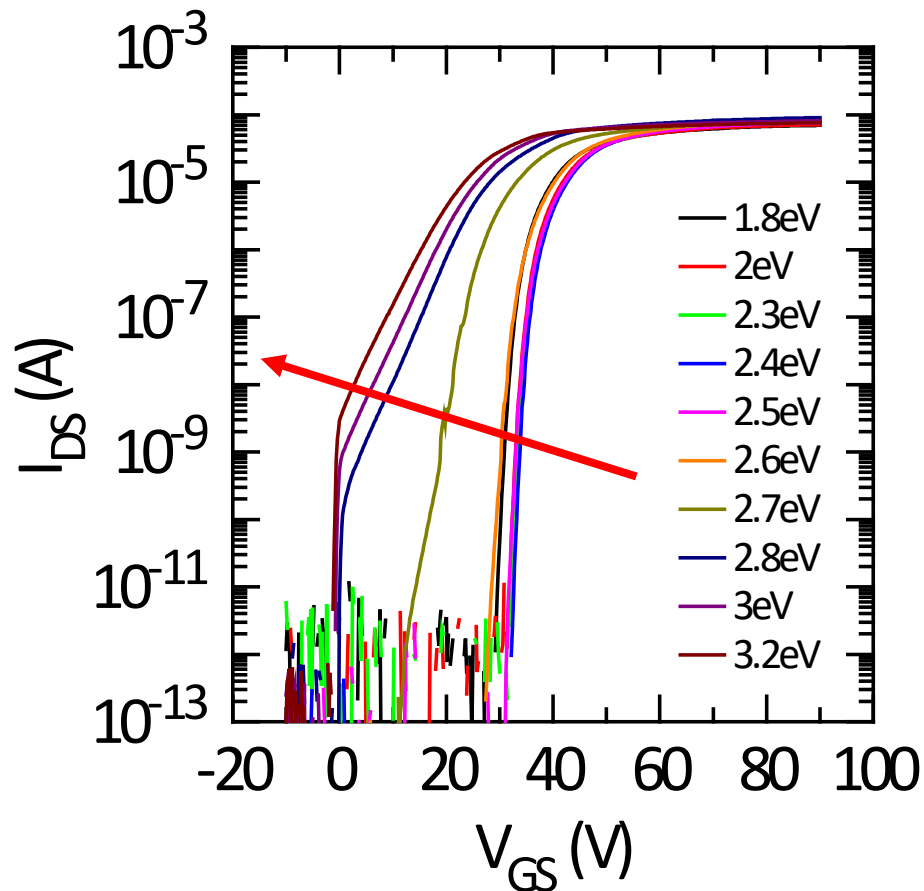
Ide et al, APL 99, 093507 (2011)
Kamiya&Hosono, ECS Trans. 54, 10 (2013)

Temperature instability

Deep traps by wb-O

Annealed at 200°C

CB

CB

E_F

E_F

O_{wb}^-

$O_{wb}^- =>$

$1/2 O_2$ (gas)+ e$^-$

e$^-$

VB

VB

Log (DOS)

Log (DOS)
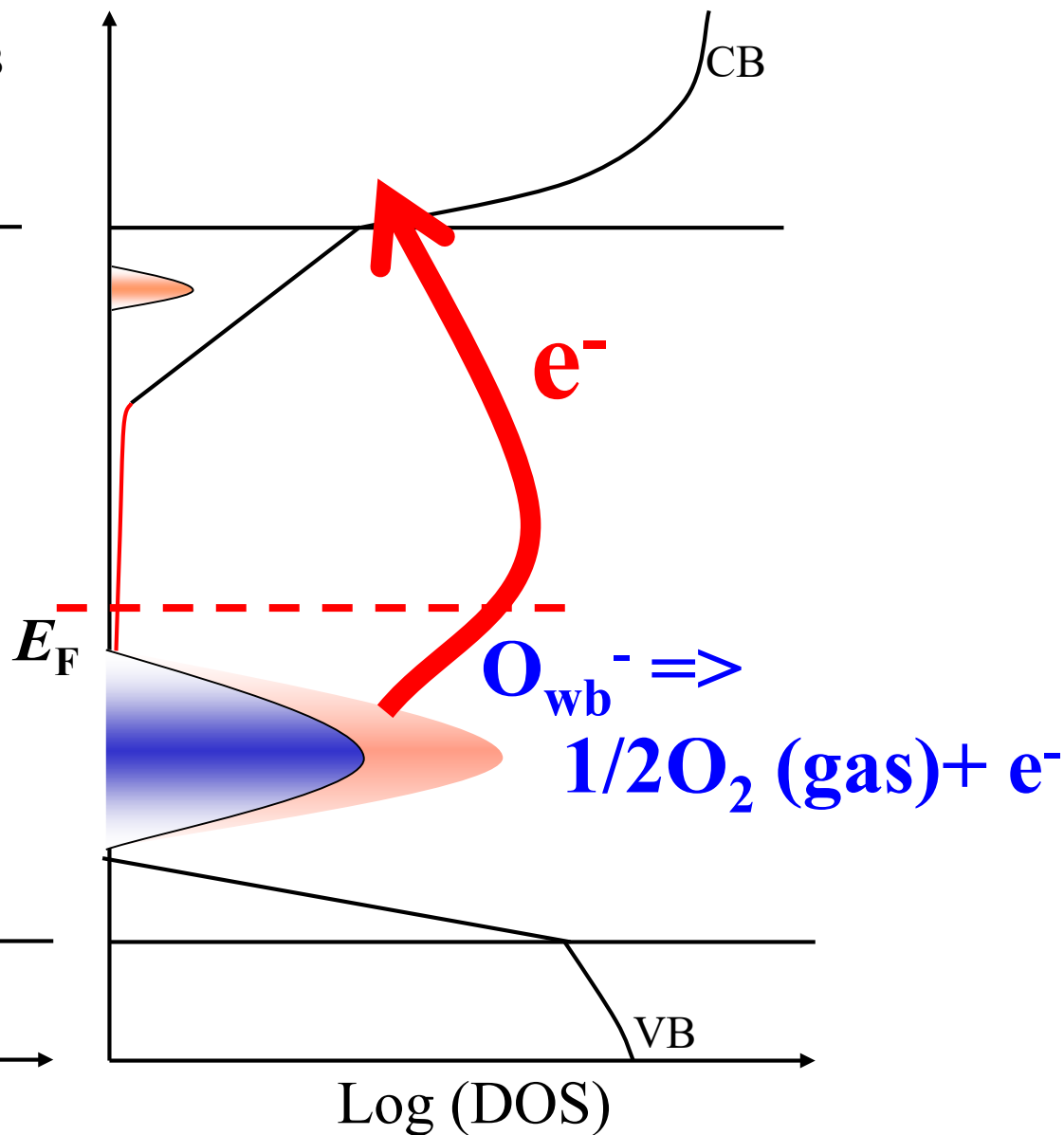
Oxygen defects in AOS

Low P_{O2}:

V_O / low-density structure
(subnanometer void)
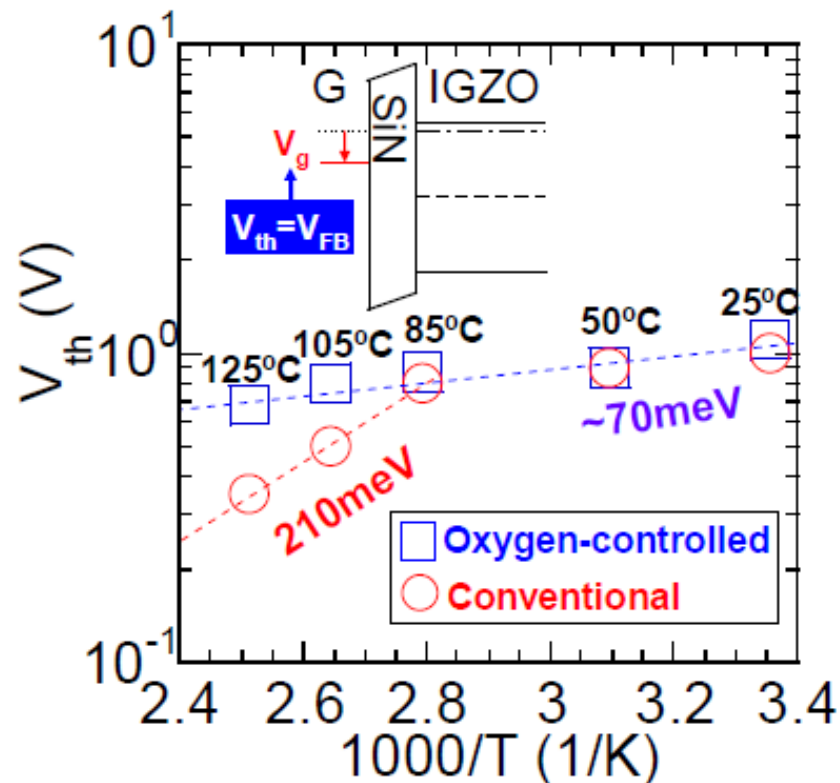traps e^- (near-VBM states)

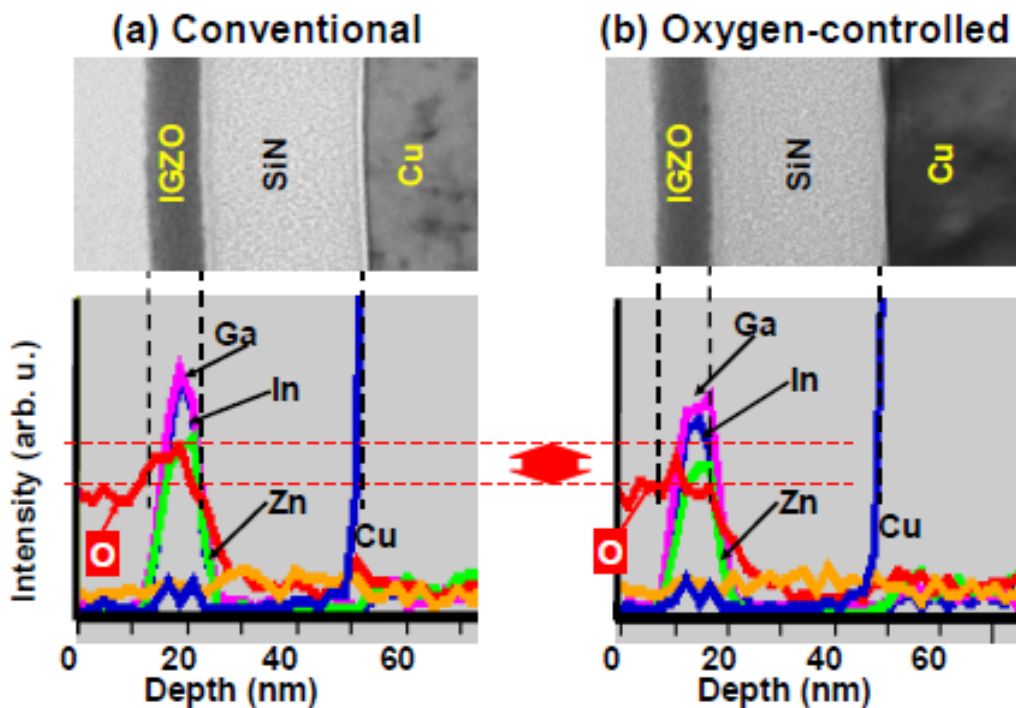**Narrow P_{O2} region
for good TFTs**

High P_{O2}:

Weakly-bonded O / Excess O
traps e^- (closer to CBM)

Oxygen stoichiometry improves stability?

Renesas electronics

**O-rich IGZO vs O-poor IGZO**

Stable up to 125°C

A Novel BEOL Transistor (BETr) with InGaZnO Embedded in Cu-Interconnects for On-chip High Voltage I/Os in Standard CMOS LSIs
K. Kaneko, N. Inoue, S. Saito, N. Furutake, Y. Hayashi, 2011 VLSI Symp. (2011) 120
Highly Reliable BEOL-Transistor with Oxygen-controlled InGaZnO and Gate/Drain Offset Design for High/Low Voltage Bridging I/O Operations
K. Kaneko et al., IEDM2011 (2011) 7.4.1
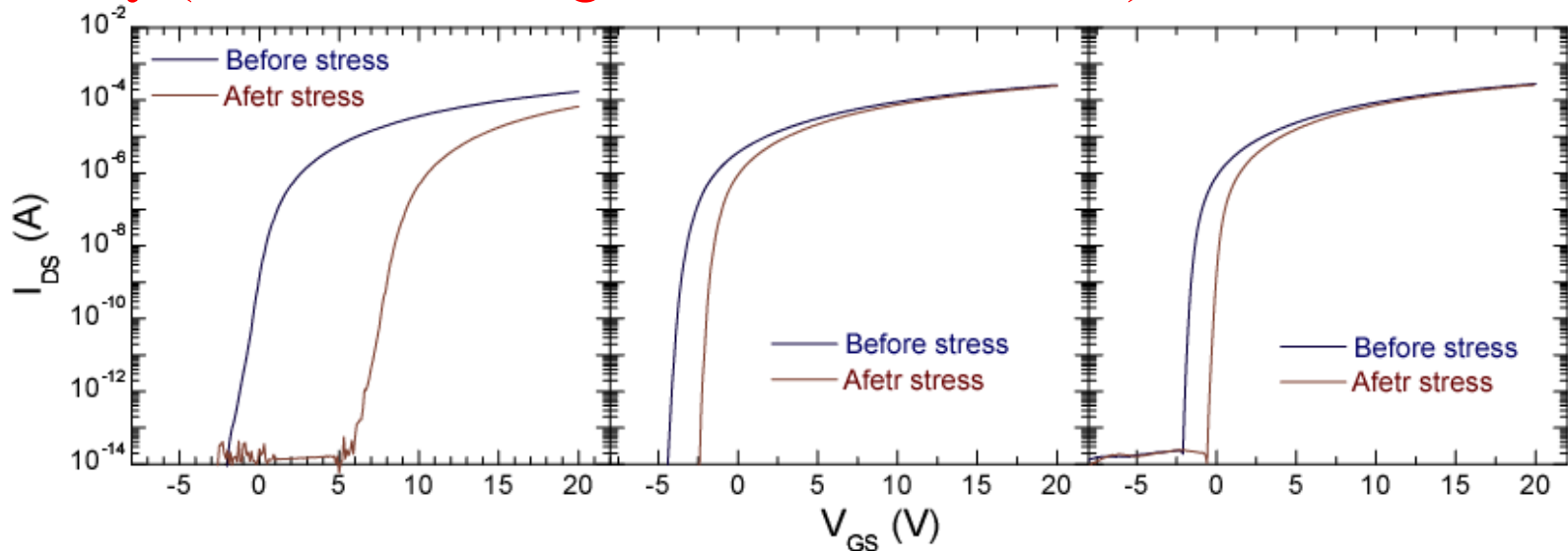
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   Weakly-bonded Oxygen
8. **Annealing**
9. Hydrogen

Hysteresis and instability in a-IGZO TFT
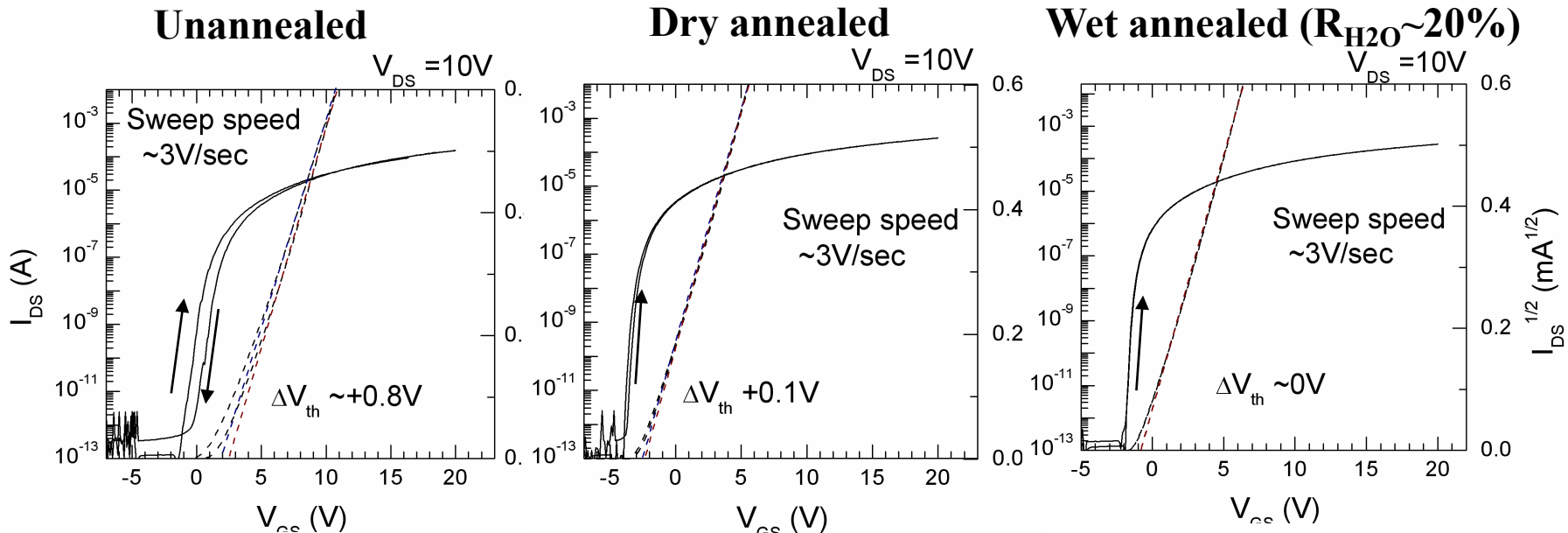
Instability (bias, current, light illumination etc…)

Effect of post-deposition annealing

HQ (High quality)
(Optimized condition)

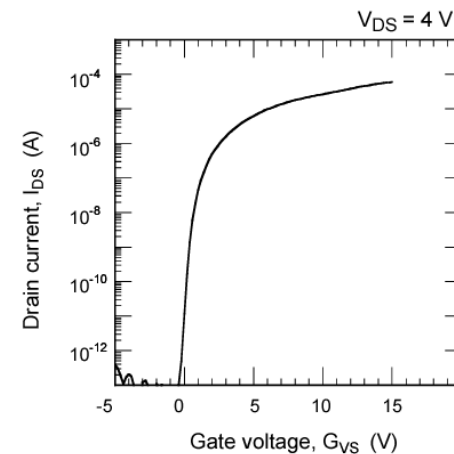**LQ (Low quality; bad condition)**

Unannealed

Unannealed

300°C annealed
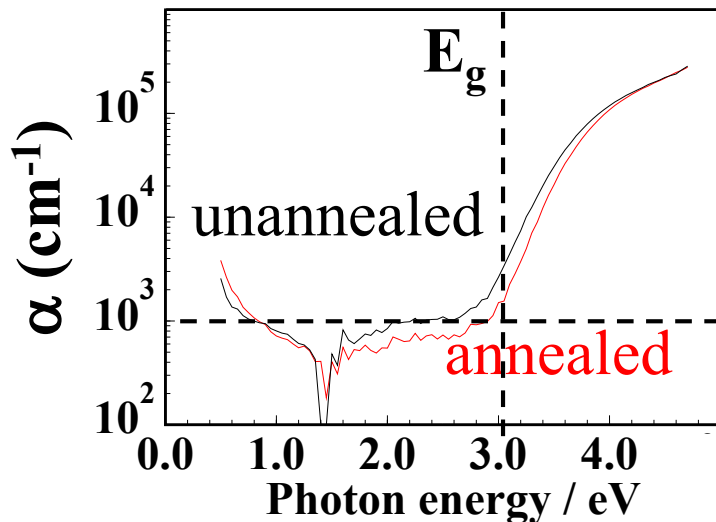
$S \sim 0.2$ V/decade
$\mu_{sat} \sim 8$ cm^2(Vs)$^{-1}$
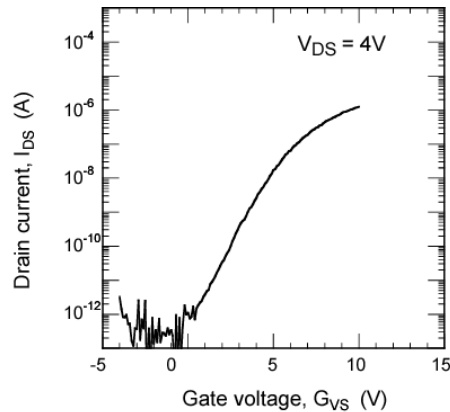
$S > 1$V/decade
$\mu_{sat} \sim 0.8$ cm^2(Vs)$^{-1}$

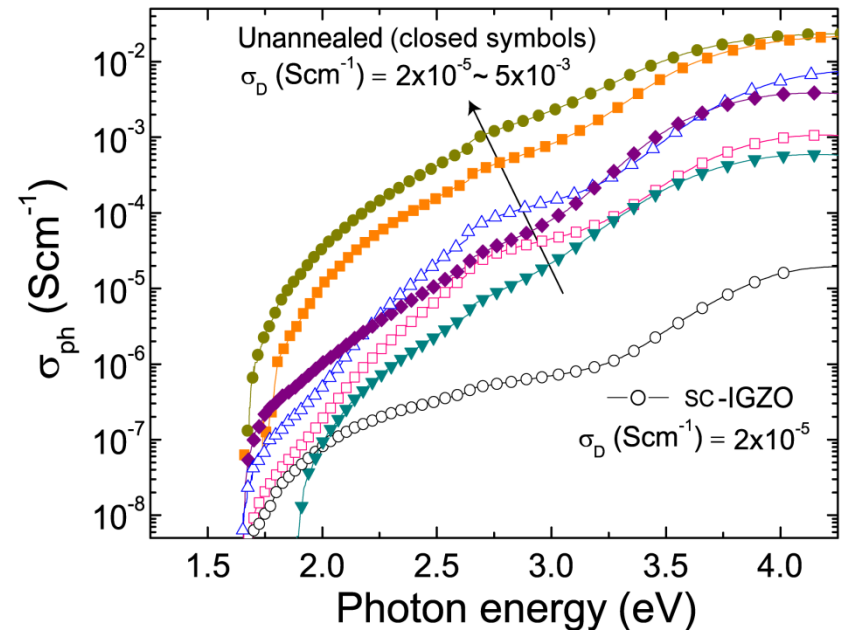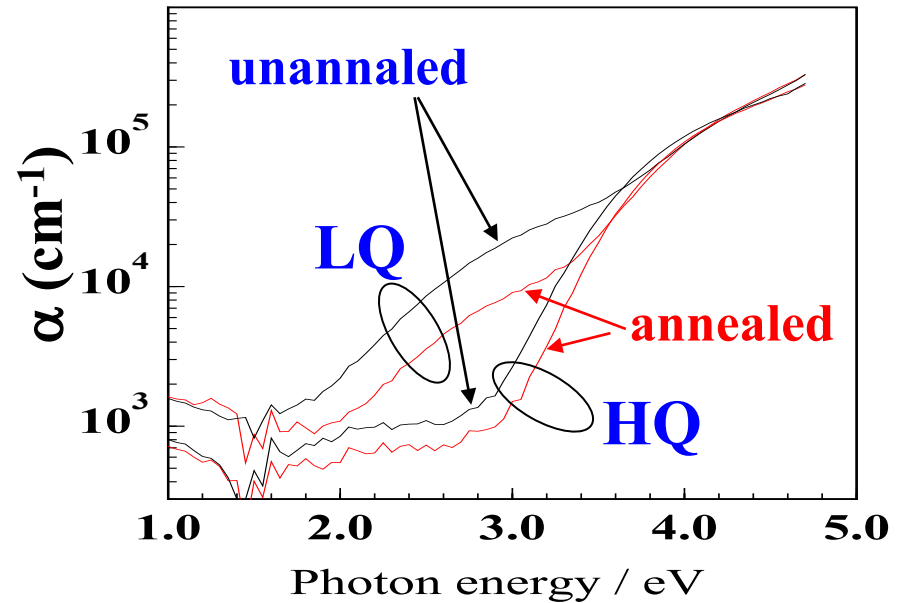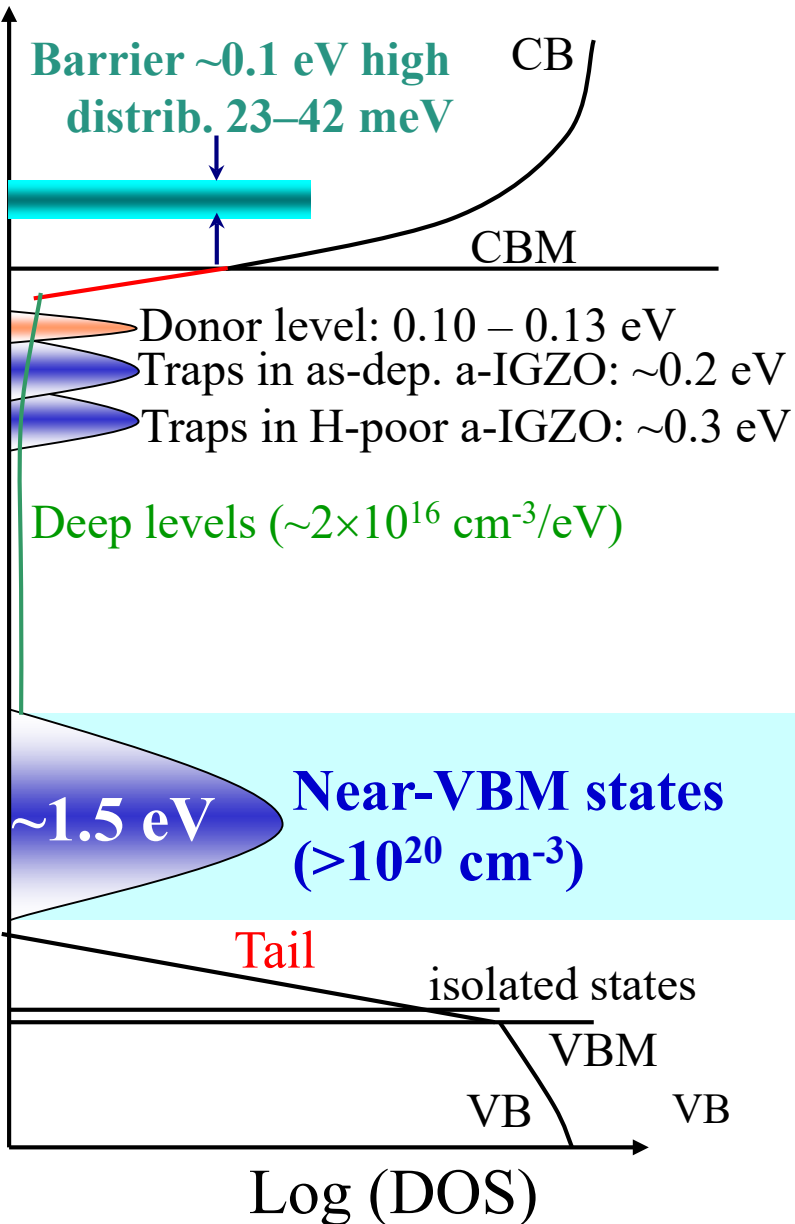$S \sim 0.2$ V/decade
$\mu_{sat} \sim 7$ cm^2(Vs)$^{-1}$
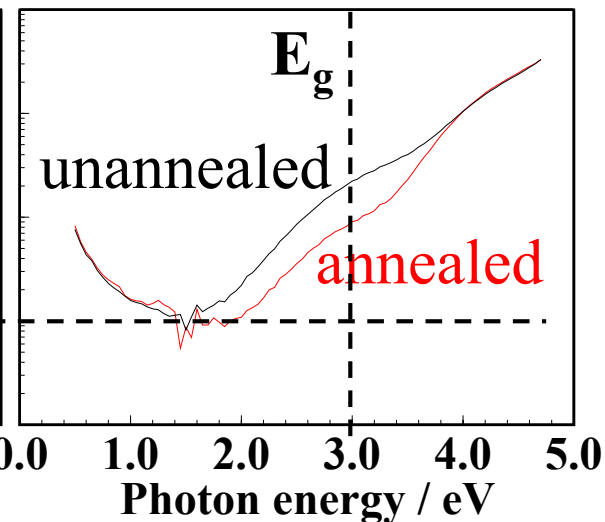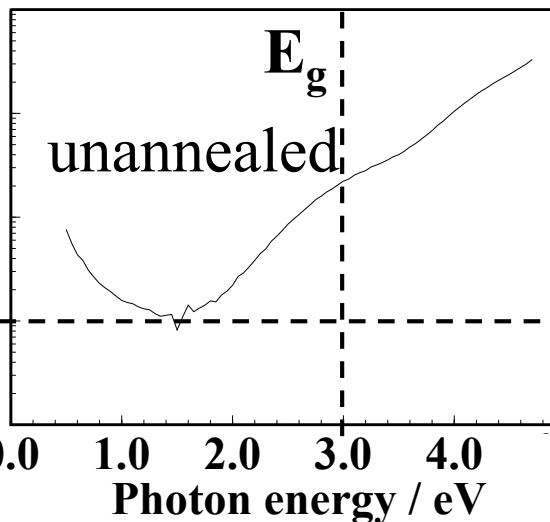
Paradoxical (peculiar) annealing effect

Annealing 'poor' TFT:

- shows an apparently good performance

- But keeps deep subgap defects

- Shallow defect states becomes similar

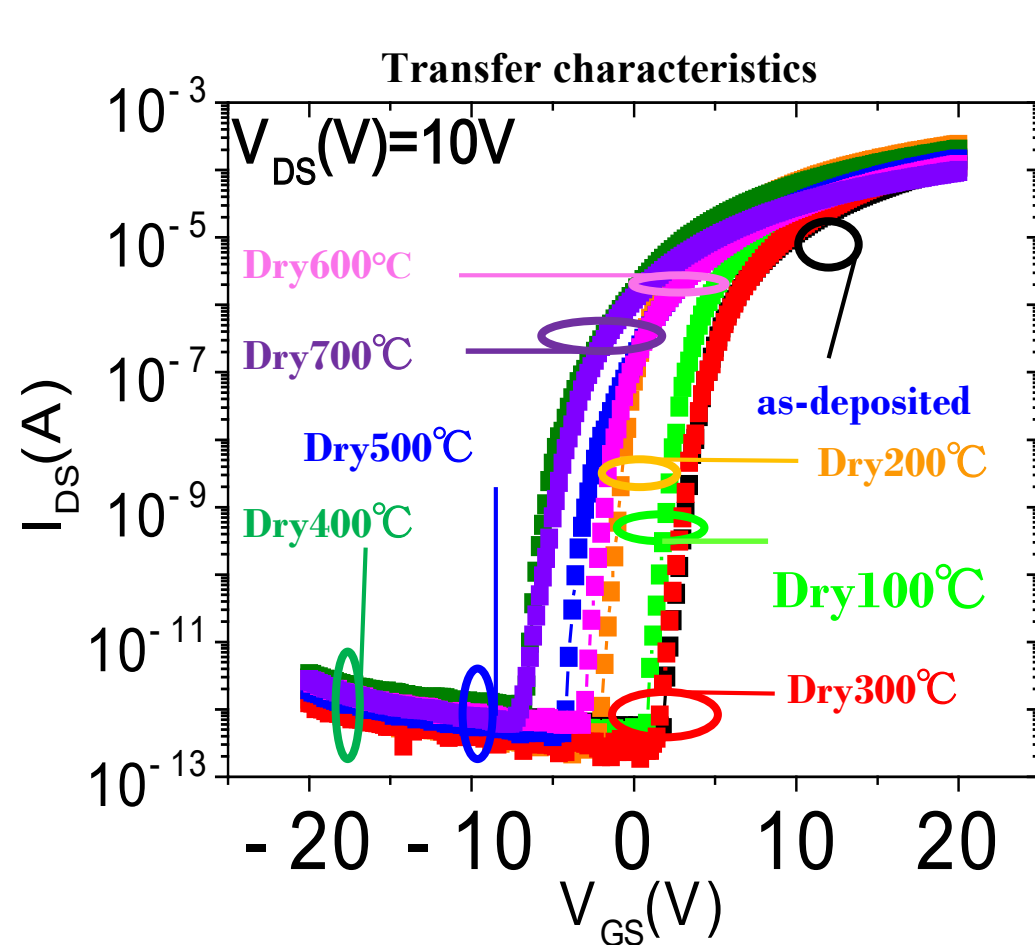- Deep defects are NOT removed by 300-400°C annealing in 'poor' TFT

=> **Important to minimize the near-VBM states in the 'AS-DEPOSITED' states**

Subgap absorption/photoresonse

Barrier ~0.1 eV high distrib. 23–42 meV

CB

CBM

Donor level: 0.10 – 0.13 eV
Traps in as-dep. a-IGZO: ~0.2 eV
Traps in H-poor a-IGZO: ~0.3 eV

Deep levels (~2×10^{16} cm^{-3}/eV)

~1.5 eV

Near-VBM states (>10^{20} cm^{-3})

Tail

isolated states

VBM

VB   VB

Log (DOS)

Subgap absorption
Photoresponse > 2.3 eV

unannaled

LQ

annealed

HQ

α (cm^{-1})

10^5

10^4

10^3

1.0   2.0   3.0   4.0   5.0

Photon energy / eV

Unanneled (closed symbols)
σ_D (Scm^{-1}) = $2\times10^{-5} \sim 5\times10^{-3}$

σ_{ph} (Scm^{-1})

10^{-2}

10^{-3}

10^{-4}

10^{-5}

10^{-6}

10^{-7}

10^{-8}

SC-IGZO
σ_D (Scm^{-1}) = 2×10^{-5}

1.5   2.0   2.5   3.0   3.5   4.0

Photon energy (eV)

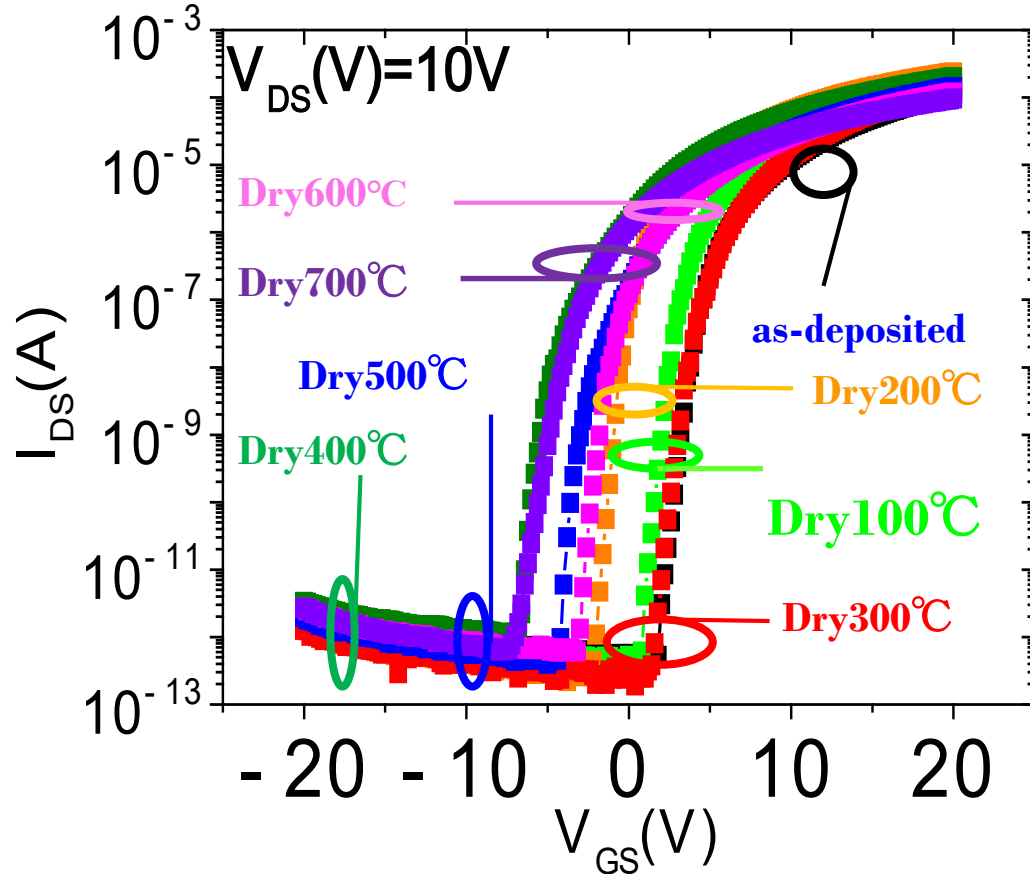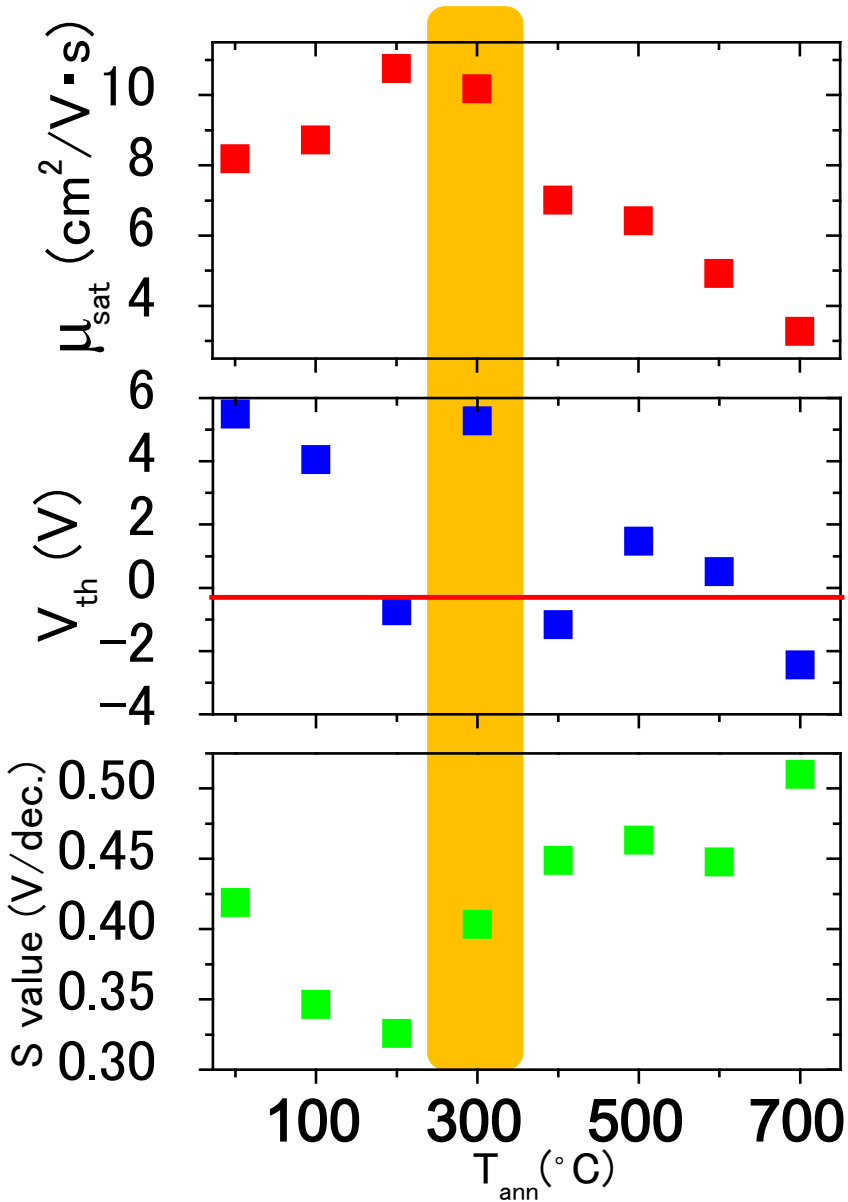# Negative Vth shift by 200°C annealing

Transfer characteristics

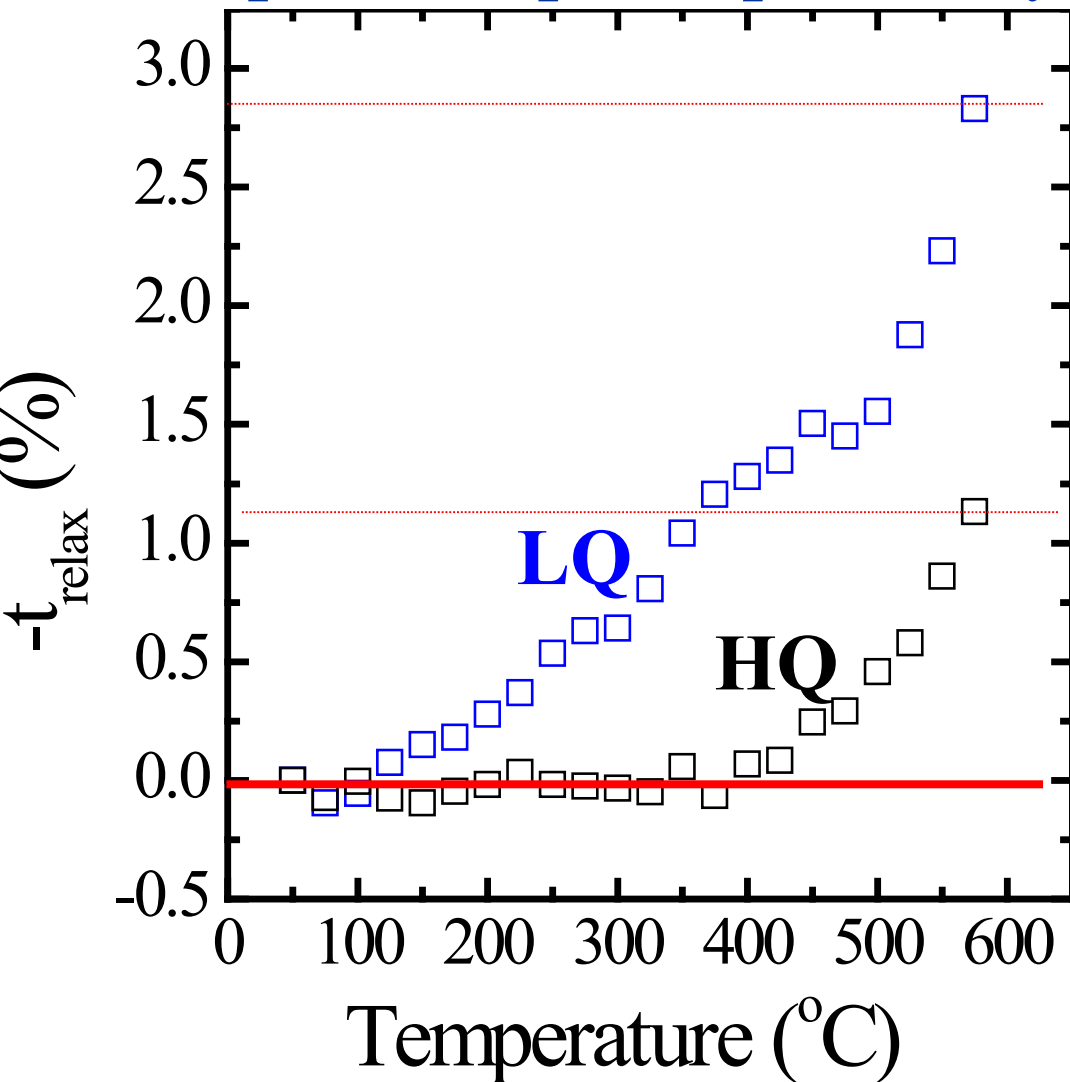TFTs annealed at >400°C exhibit poorer characteristics
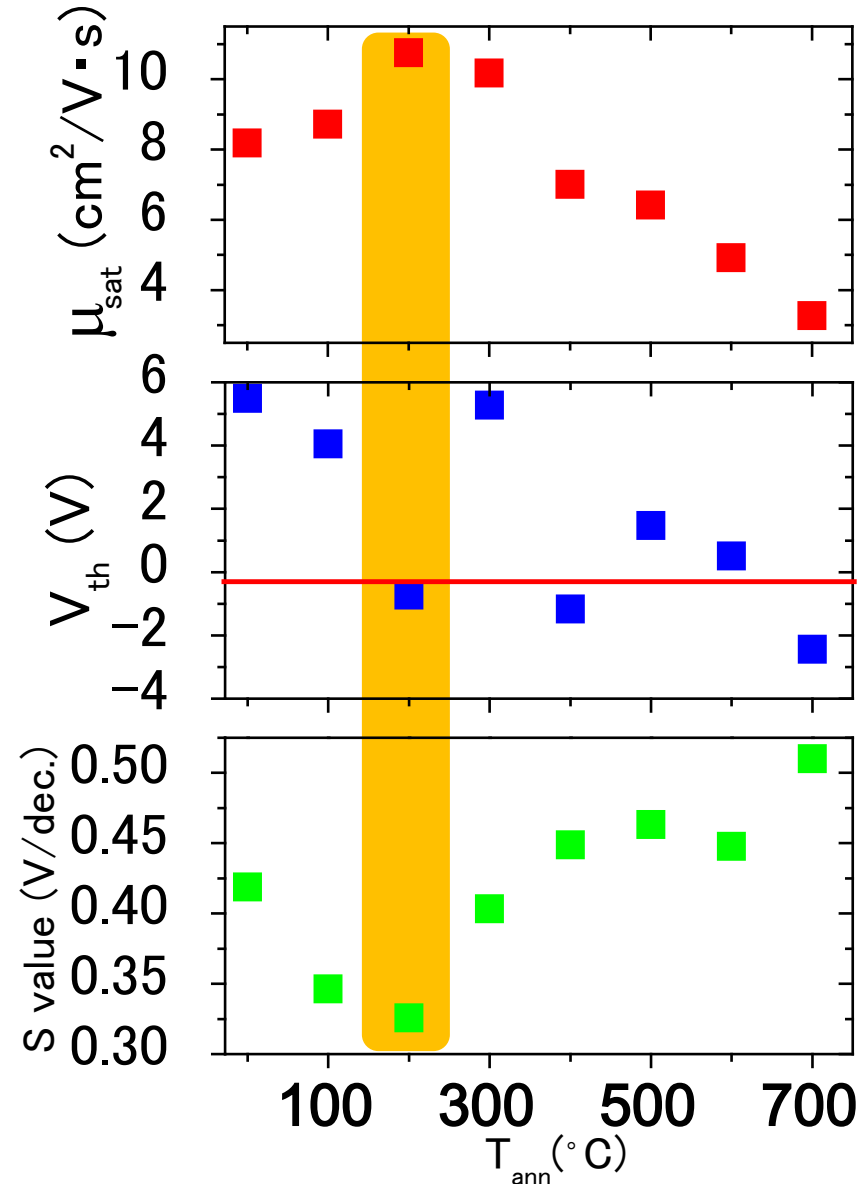
What happens at 300-400°C?

Y. Hanyu et al., J. Displ. Technol. **10,** 979 (2014)

Structural relaxation during annealing

In-situ spectroscopic ellipsometory

HQ:
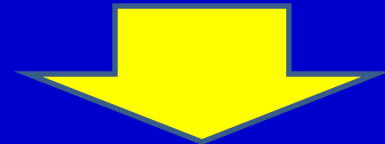   No detectable relaxation
   up to 400°C

LQ:
   Relaxation start from
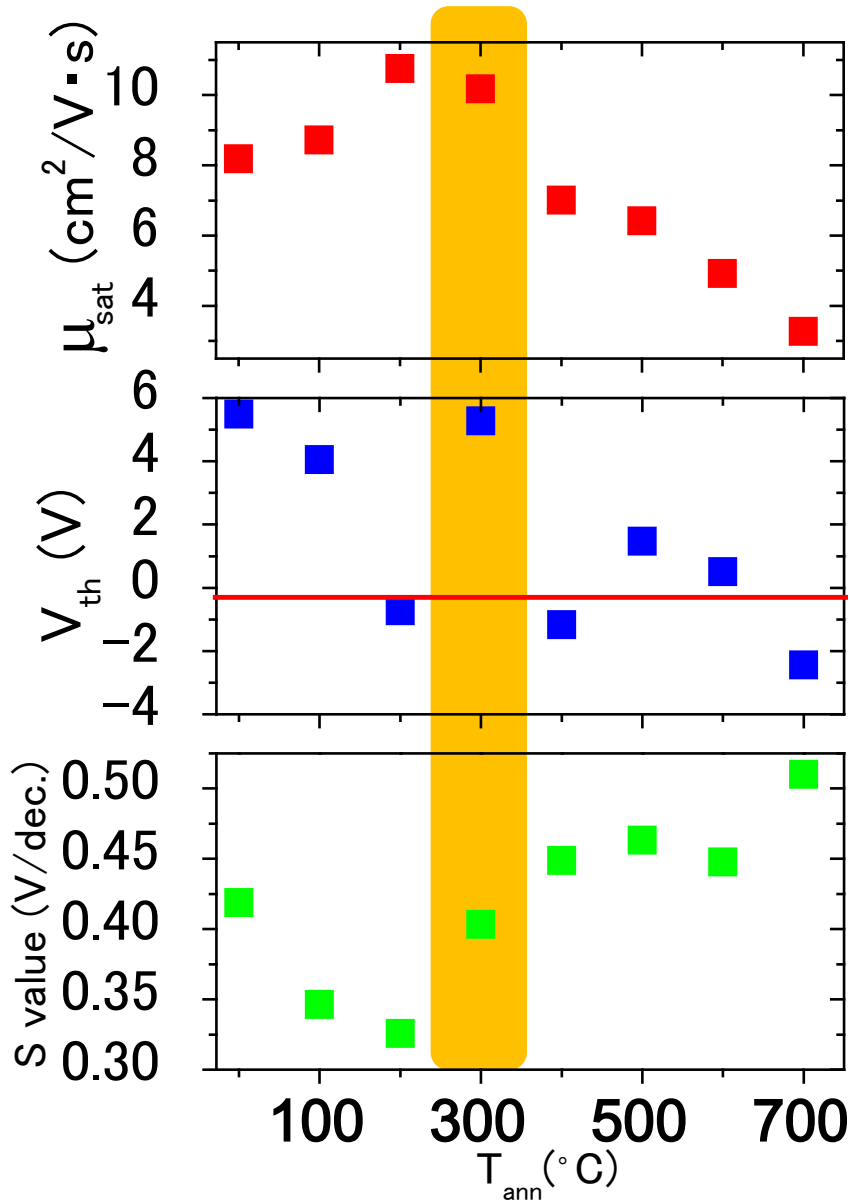   **100°C**
   Larger densification

   Low density
   Poor structural stability

Ide et al, JAP 111, 073513 (2012)

Kamiya&Hosono, ECS Trans. 54, 10 (2013)

What happens at 300-400ºC?

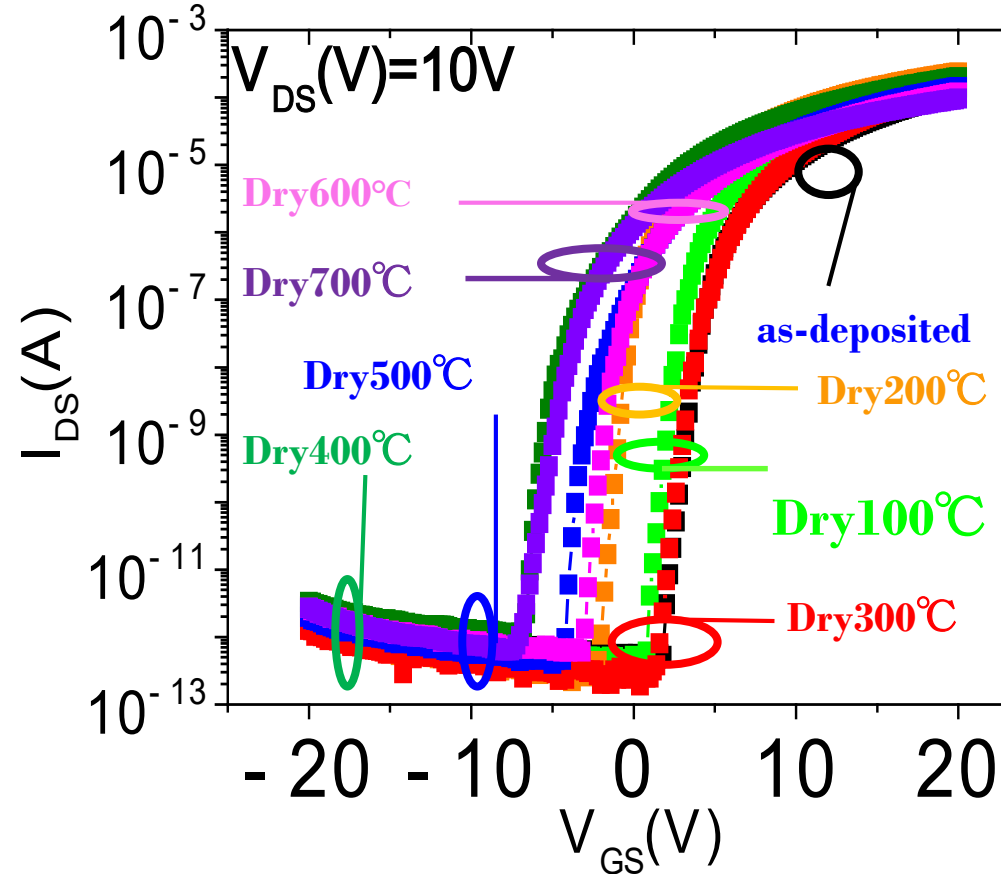**No detectable structure relaxation**

Annihilation of point defects (e.g. by oxygen diffusion)

What happens at 400 – 500°C?
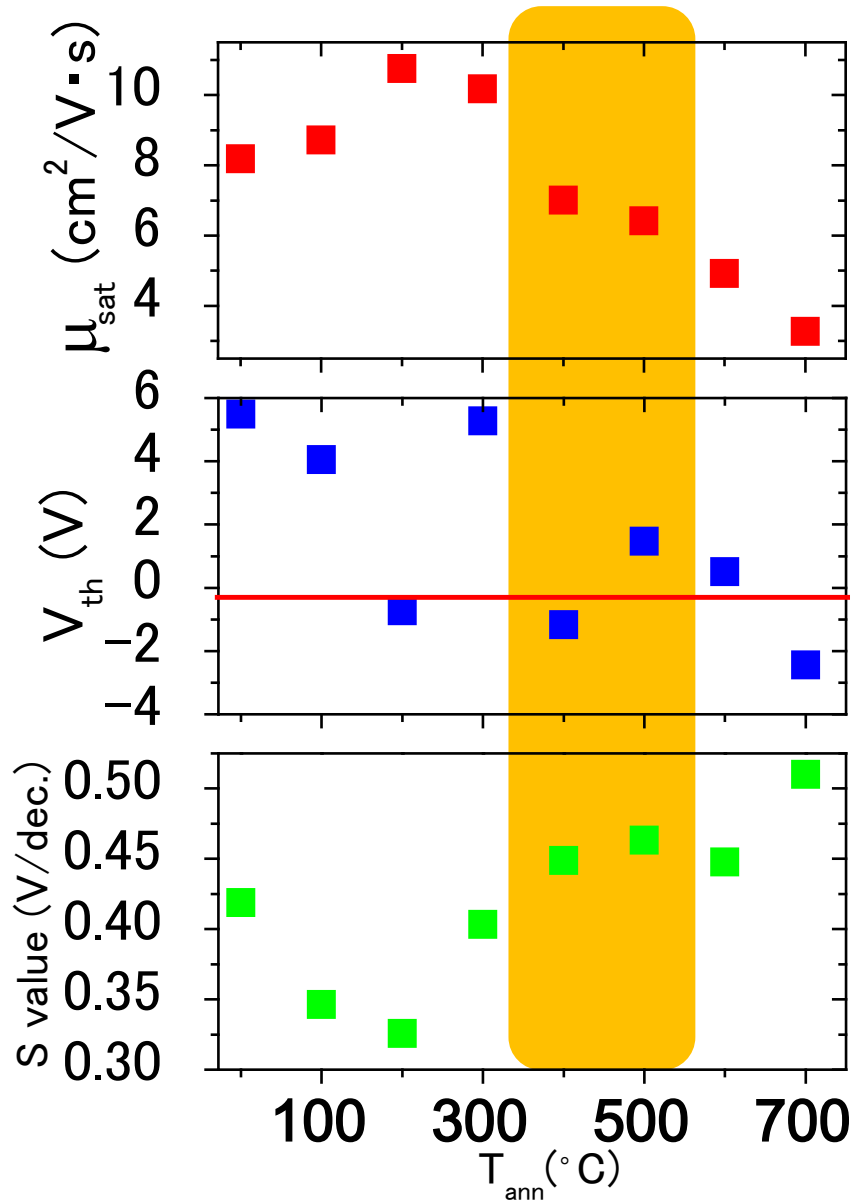
Thermal desorption spectra (TDS)

Annealed $\geqq 400°C$: Poor TFT

H_2O (M/z = 18)

Po$_2$ 4%

Po$_2$ 2%

Po$_2$ 3%

Temperature (℃)

Dry anneal @500°C
(H depletion)
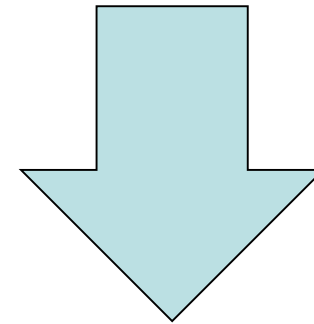
Re-dope hydrogen:
H_2 plasma treatment
Dry H_2 anneal
Wet O_2 anneal

H re-doping after 500ºC O$_2$ annealing

Y. Hanyu et al., J. Displ. Technol. **10,** 979 (2014)

Transfer characteristics

TFT parameters vs ann. cond.
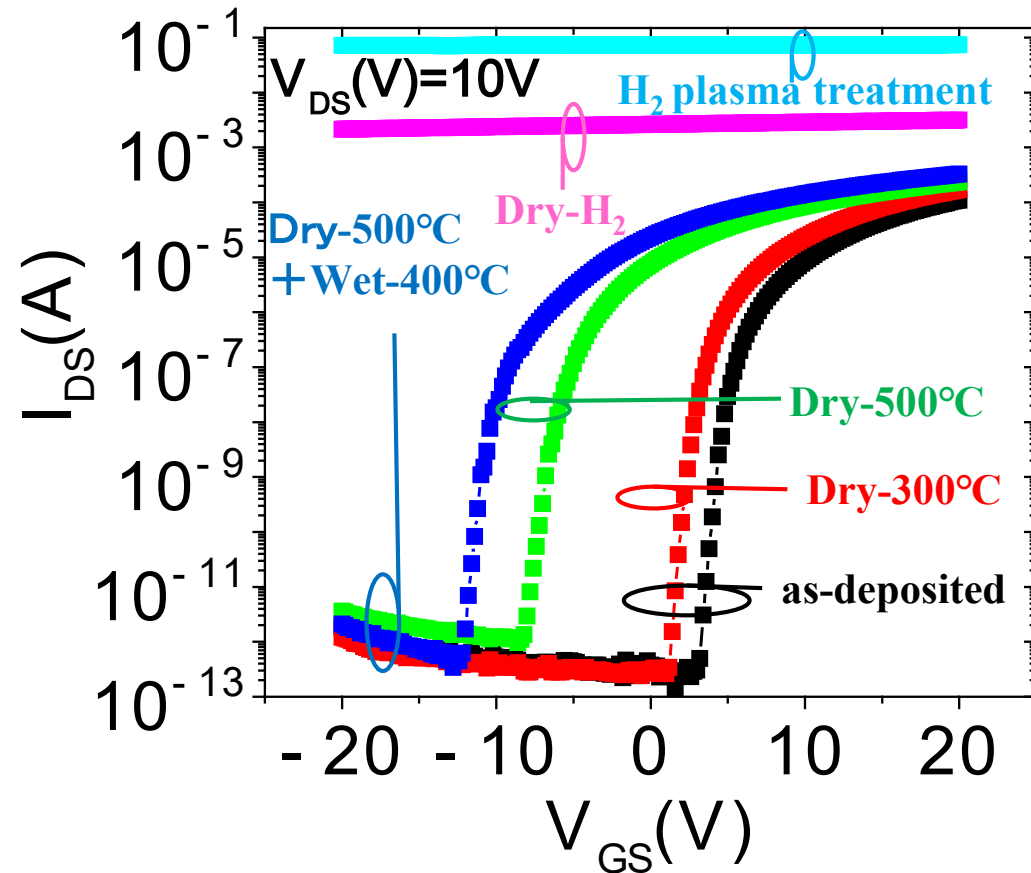
H$_2$ plasma & dry H$_2$ anneal: No turn-off
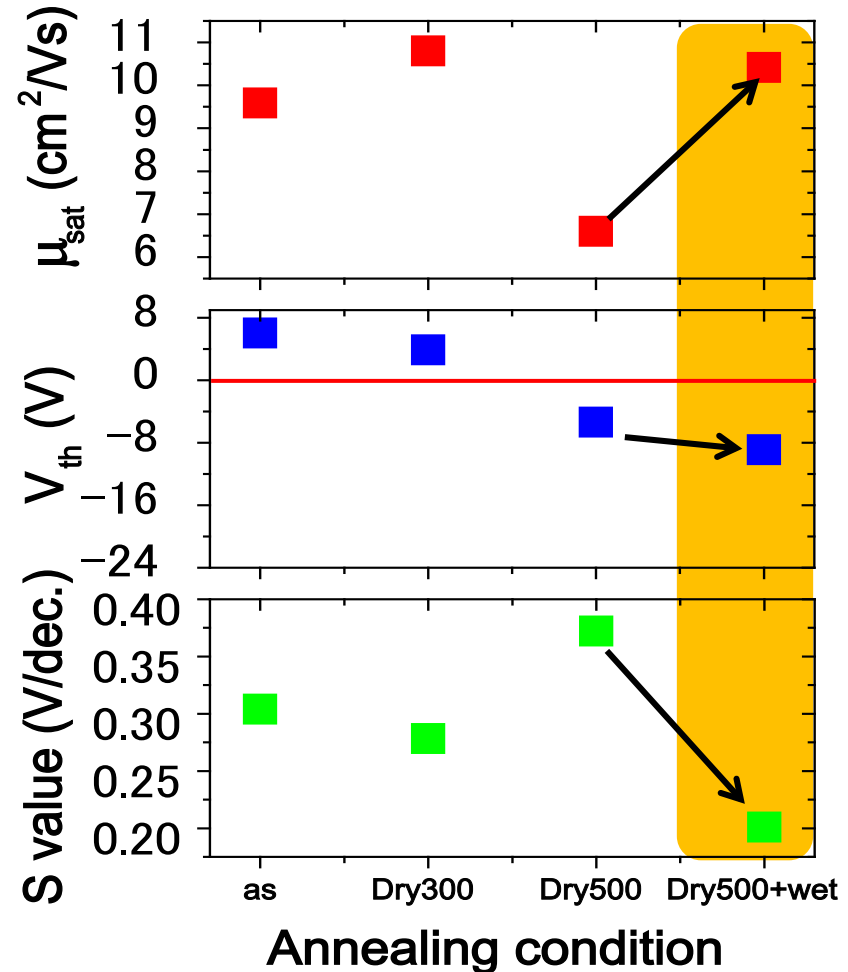
H re-doping after 500°C O₂ annealing

500°C O₂ annealing (H depletion)
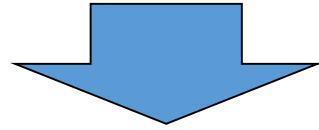
H re-doping by O₂+H₂O annealing
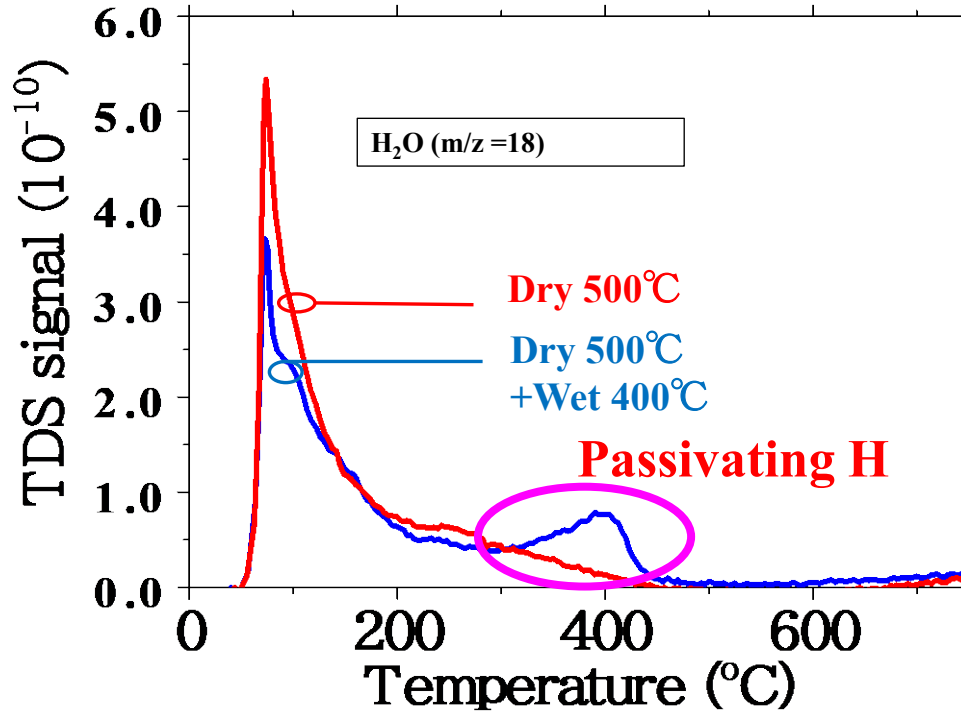
Variation of TFT parameters
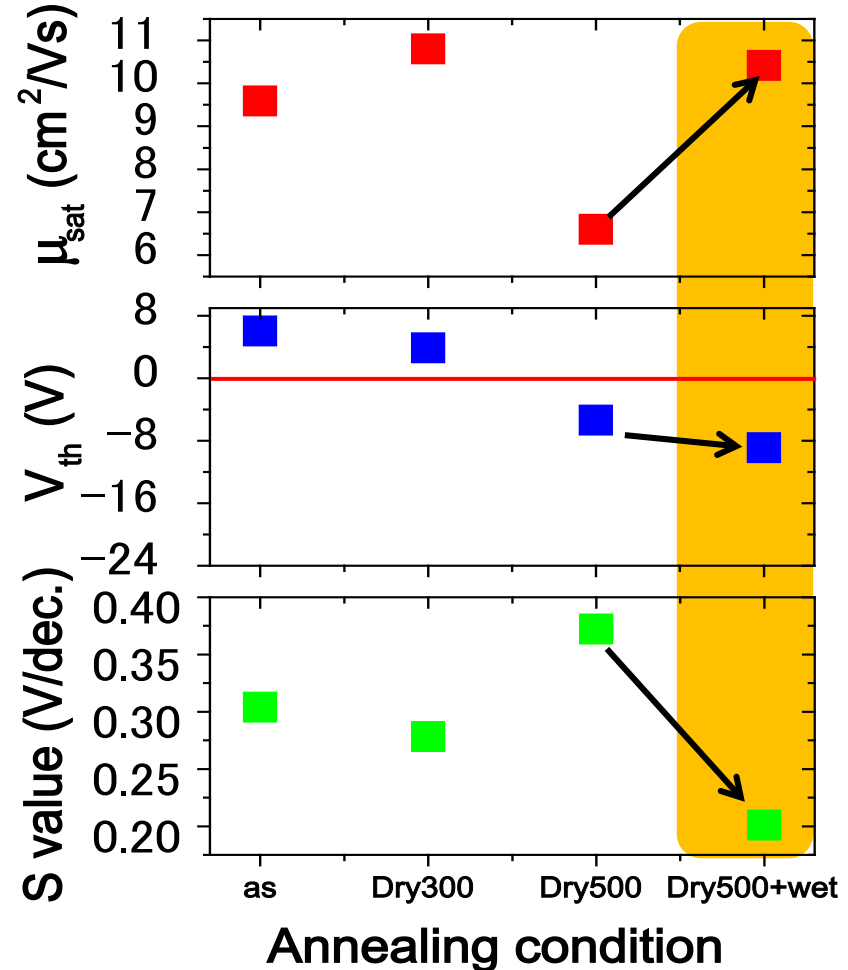
Evidence of H passivation in a-IGZO

By thermal annealing…

1. **<200ºC**   : **Deep traps decrease / donor decreases**
     but no densification
       Desorption of weakly-bonded oxygen / H (H_2O)
        increases free electrons

2. **100 – 300ºC:** E_g **increases (reduction of tail states)**

3. **300 – 400ºC: Donors decrease (Oxidation)**
      Hysterisis / stability improved

4. **>400ºC**   : **H depletion (depassivation)**
     Deteriorated mobility / TFT

5. **300 – 600ºC: Densification (structural relaxation)**

6. **600ºC**   : **Crystallization**

7. **Low-quality, low-density a-IGZO show a large densification**
     from 100ºC by ~4 %
      (*cf.* **>400ºC, 1% for HQ a-IGZO)**

CONTENT for AOS TFT

1. Characteristics of a-IGZO TFT
2. Current AOS displays
3. Materials
4. Growth condition and TFT fabrication
5. Doping
6. Defect structures (subgap defects)
7. Why too large P_{O2} is bad?:
   Weakly-bonded Oxygen
8. Annealing
9. Hydrogen

Electron doping by post-dep H treatments

K. Nomura, ECS JSS **2**, P5 (2013)

H$^+$ implantation @RT

Annealing in N$_2$:H$_2$ = 97:3

a-IGZO
< 10^{16}
~ 10^{20}

c-IGZO
< 10^{16}
~ 10^{20}

α (10^5 cm^{-1})

Photon energy (eV)

Carrier density (cm^{-3})

Annealing temperature (K)

H plasma @RT

Carrier concentration (cm^{-3})

Hall mobility μ_H (cm^2 / Vs)

N_e

μ_H

@300K

Film thickness (nm)
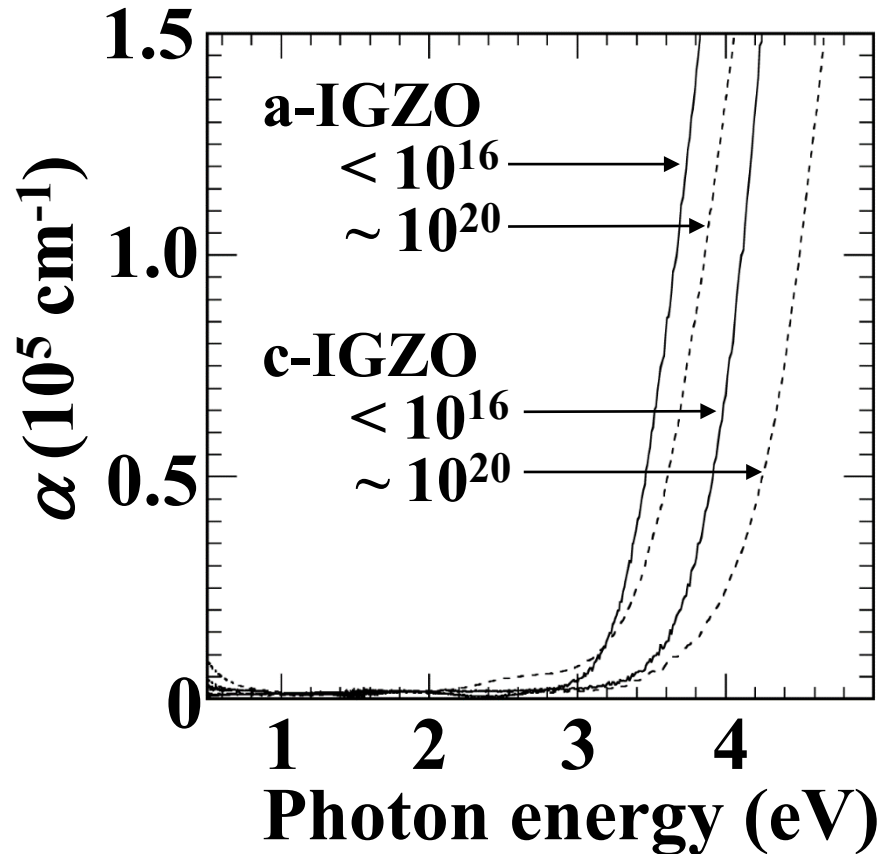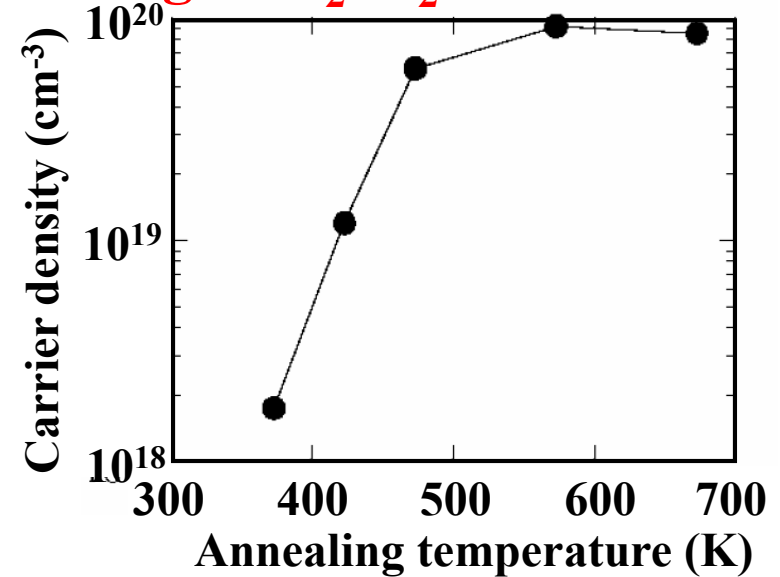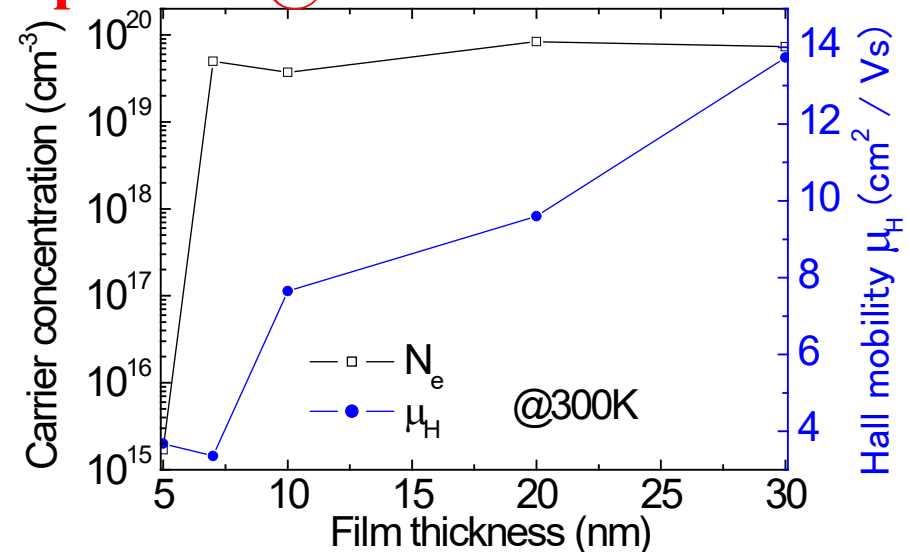
H in a-IGZO

T. Kamiya et al., phys. stat. sol. A **207**, 1698 (2010)

Zn

H bonded to 3 fold coordinated O
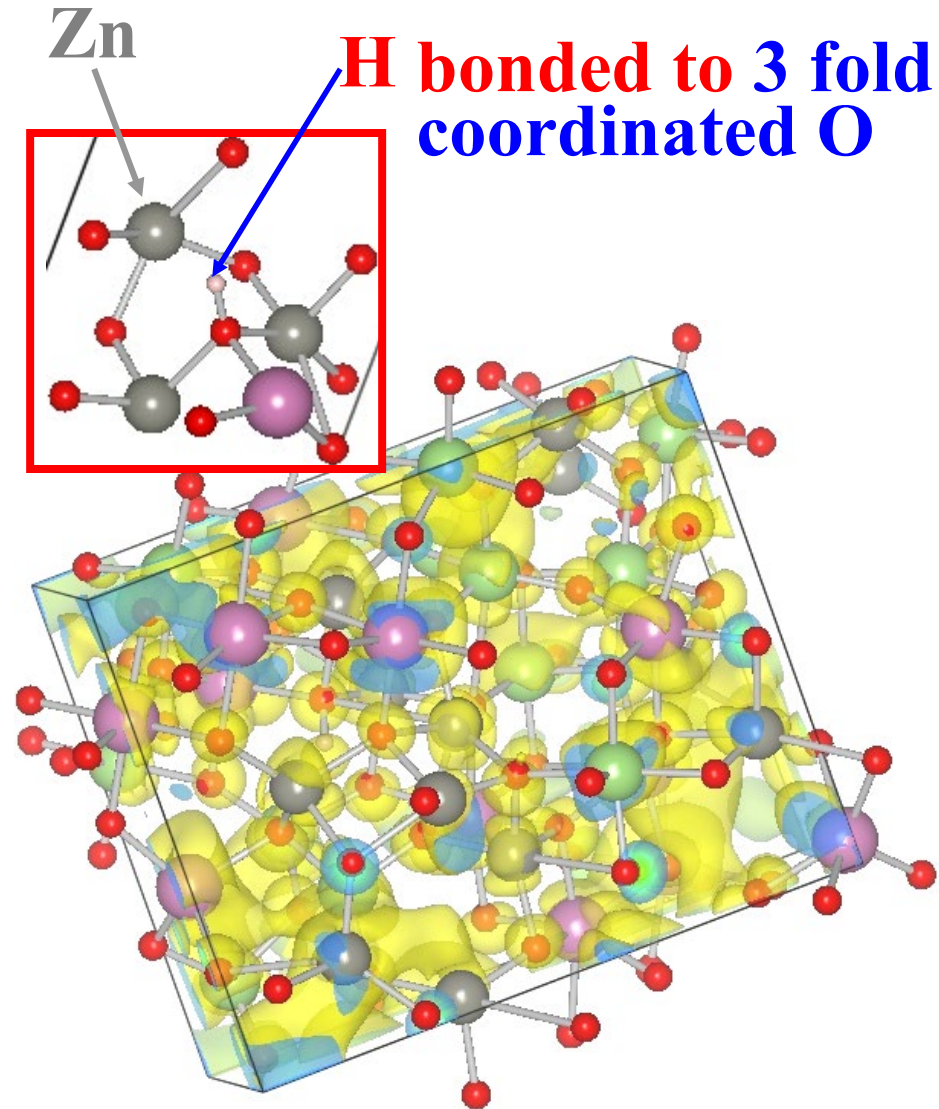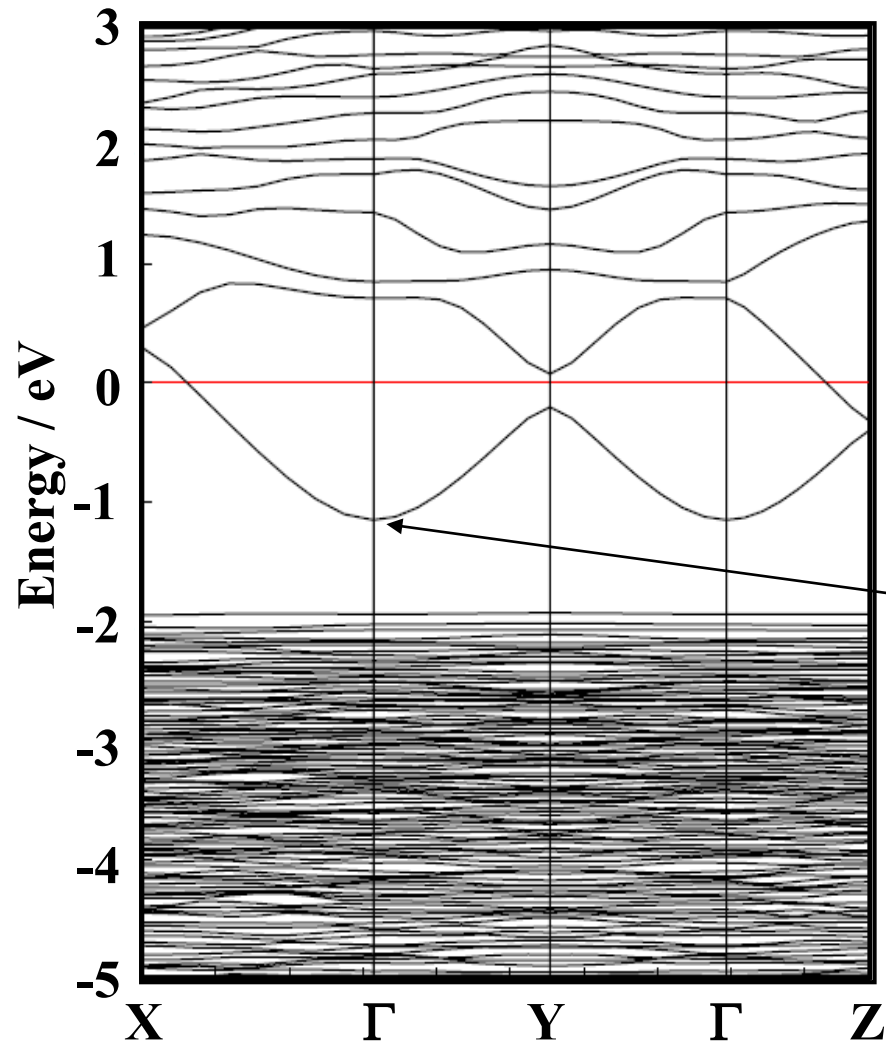
O-H in H_2O: 0.097 nm

Hydrogen doping in ZnO
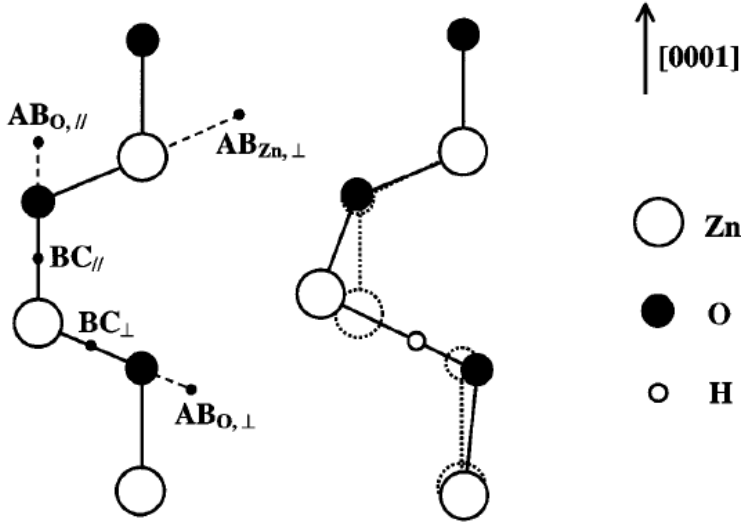
Charge state	Location	E^f (eV)
H^+	$BC_\perp$	-1.84
H^+	$BC_\parallel$	-1.82
H^+	$AB_{O,\perp}$	-1.78
H^+	$AB_{O,\parallel}$	-1.59
H^0	$BC_\perp$	1.07
H^-	$BC_\perp$	3.92
H_2	$AB_{Zn,\perp}$	0.84
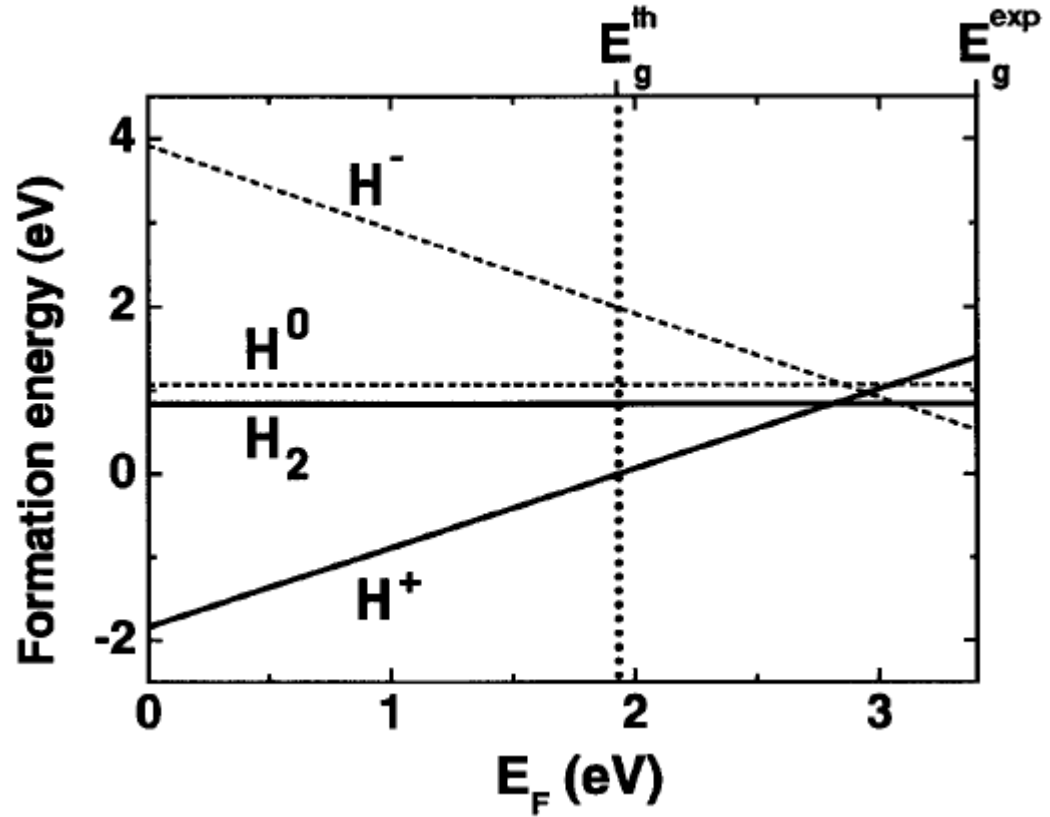
FIG. 2. Formation energies of interstitial hydrogen in ZnO, as a function of Fermi level, obtained from DFT-LDA calculations and referenced to the energy of a free H_2 molecule. For each charge state, only the lowest-energy configuration is shown. Zero-point energies are included. The zero of Fermi energy is chosen at the top of the valence band, and both the *theoretical* (E_g^{th} = 1.91 eV, dotted line) and *experimental* (E_g^{exp} = 3.4 eV) band gaps are indicated. The energies for H^0 and H^- are shown in dashed lines to indicate they are underestimated in the LDA calculations; after correction, H^+ is the lowest-energy state throughout the experimental band gap.

Chris G. Van de Walle, Hydrogen as a Cause of Doping in Zinc Oxide, Phys. Rev. Lett. 85, 1012 - 1015 (2000)

Hydrogen is donor?

Deposited by PLD

[H] by SIMS   **[H]**   **N_e**
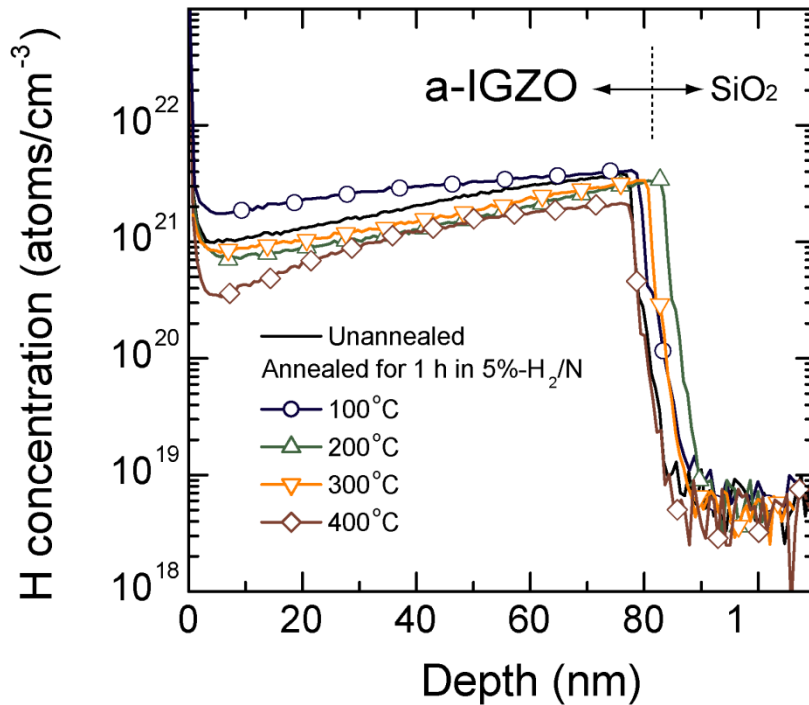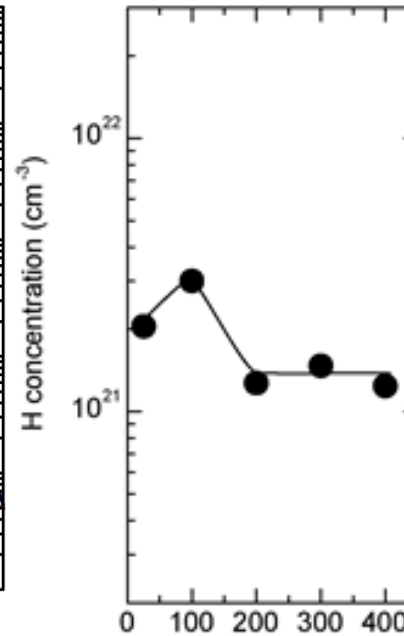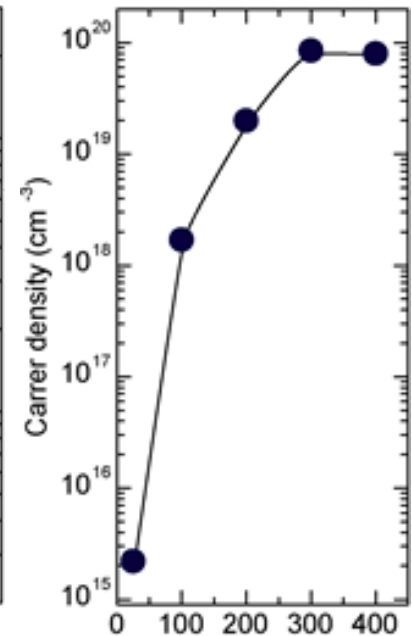
Model: Donor hydrogens are compensated by excess oxygen

No H_2, H_n by Raman / –OH detected by IR

K. Nomura, ECS JSS **2**, P5 (2013)

$(N_e \sim 10^{15} \text{cm}^{-3})$

ATR-FTIR
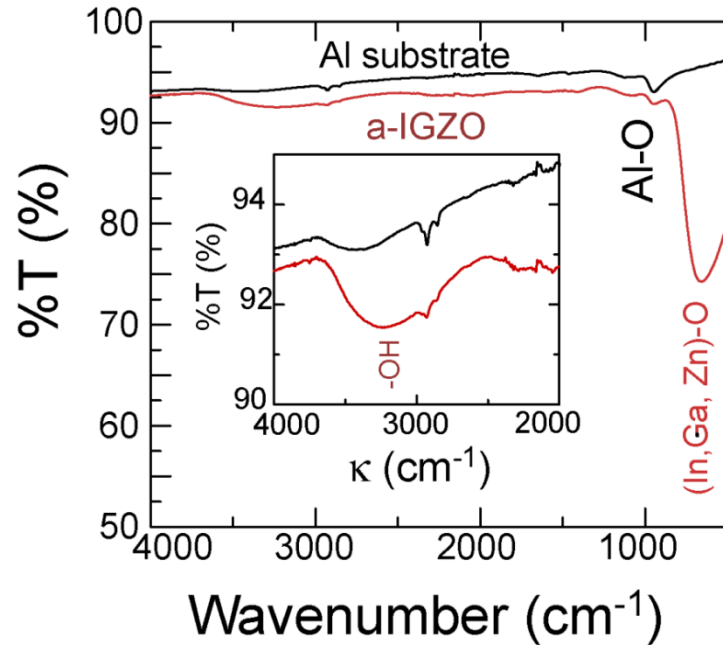
Raman

(Detection limit for H_2 : $2 \times 10^{18} \text{cm}^{-3}$)
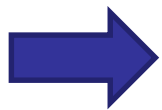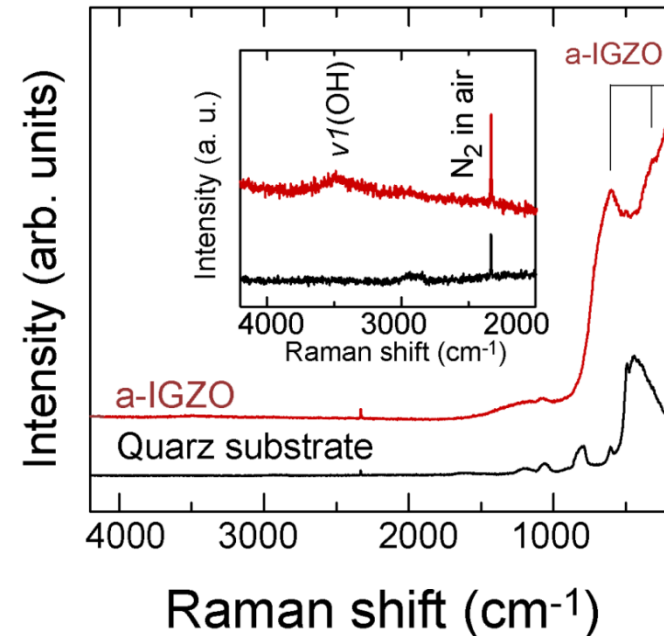
➡ **Hydrogen mainly exists as –OH species, which is expected to work as a donor.**

Doping to a-IGZO by H treatments: O 1s spectra

Optimum R_{O2} = 3%, 6 keV HAXPES

As-deposited

H treated

HT H$_2$
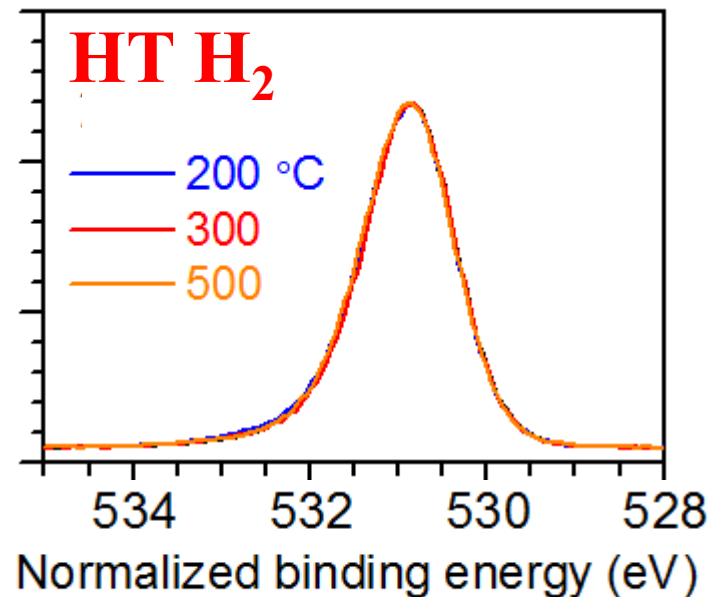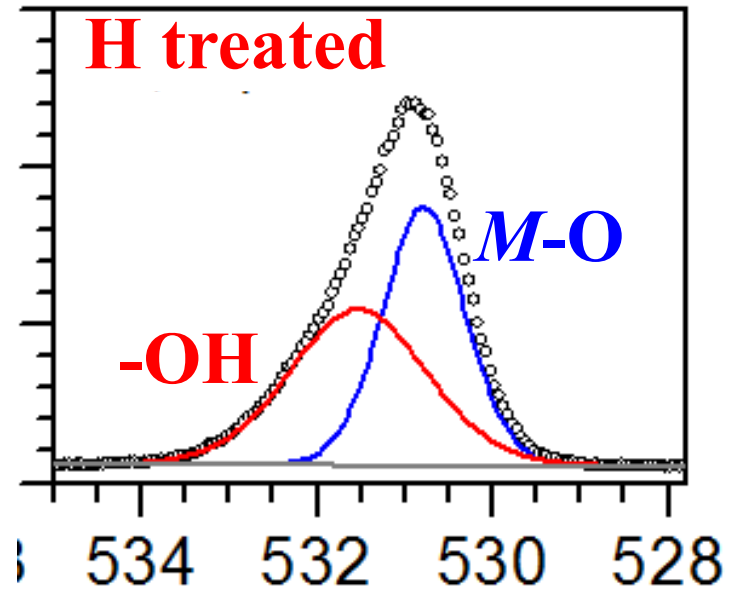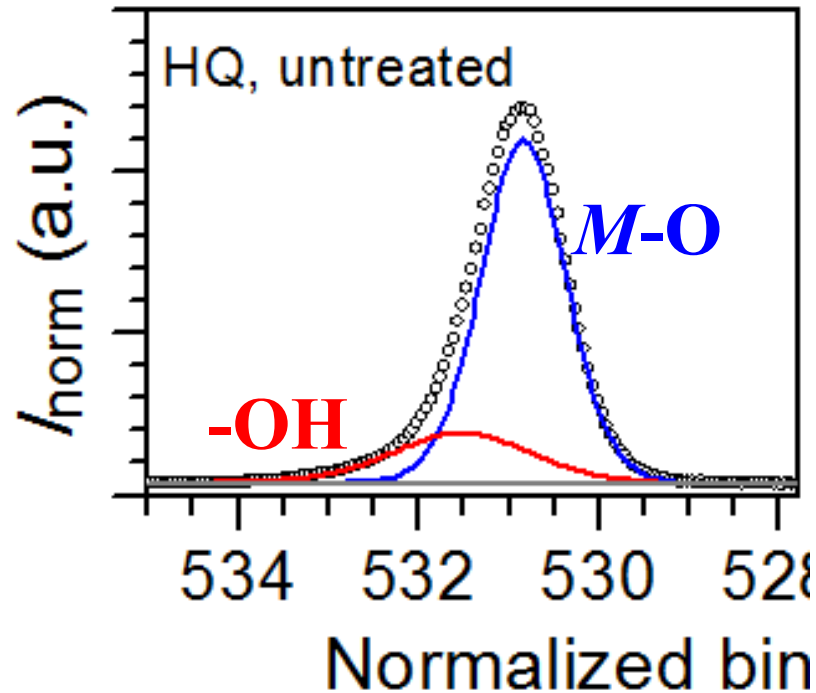
H treatment:
RT: H doping, -O^{2-}H^{+} + e^{-}
HT: Reduction, V$_O$$^{2+}$ + 2e^{-}

-O²⁻H⁺ and H⁻ in STD sputtered a-IGZO

Hydrogen anion and subgap states in amorphous In–Ga–Zn–O thin films for TFT applications
J. Bang et al., Appl. Phys. Lett., **110**, 232105 (2017).

DFT (phonon)

IR/Raman for 2 μm-thick film

-O²⁻H⁺ : H⁻ ~ 2 : 1
-OH is stable only up to ~600 °C (crystallization)
H⁻ is much stable even after crystallization up to >800°C

H donors compensated by excess O

Stoiciometric a-IGZO:

$$2 \text{ -M-O} + 2\text{H} + \textcolor{red}{0 \text{ e}^-} \Rightarrow 2 \text{ -M-O-}\textcolor{red}{\text{H}^+} + \textcolor{red}{2 \text{ e}^-}$$

**No way to make 'stoichiometric' amorphous film.
'Best' chemical composition is chosen
                based on electrical properties.**

O-rich a-IGZO:

$$2 \text{ -M-O} + 2\text{H} + \textcolor{red}{1/2\text{O}_2} + \textcolor{red}{0 \text{ e}^-}$$
$$\Rightarrow \text{-M-O-}\textcolor{red}{\text{H}^+} + \textcolor{red}{\text{-O}^{2-}}\text{-M-O-}\textcolor{red}{\text{H}^+}$$
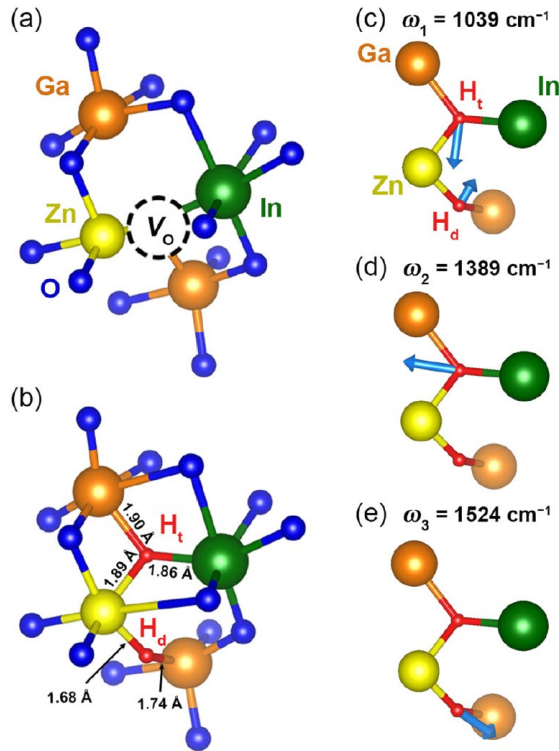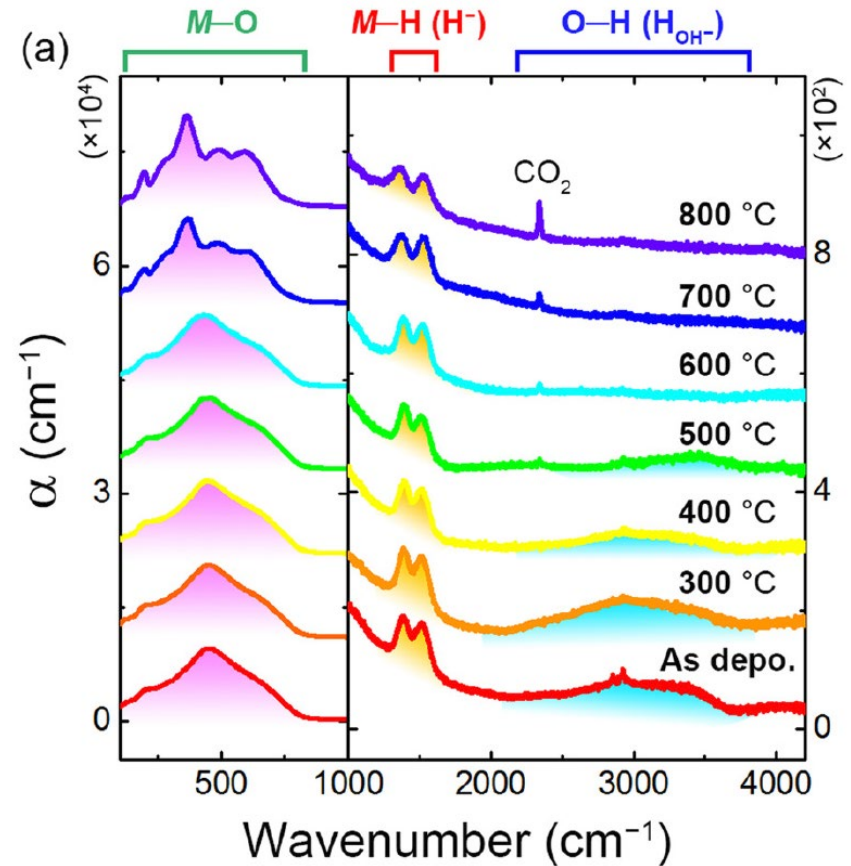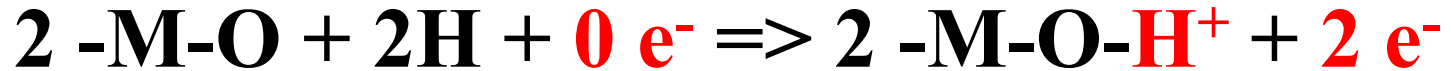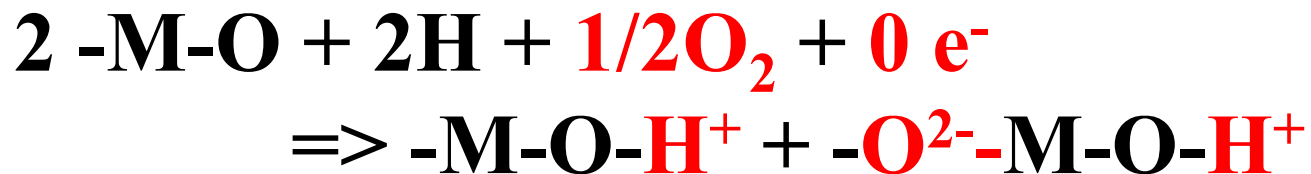
O₂ supply is necessary for STD sputtering

Conductivity
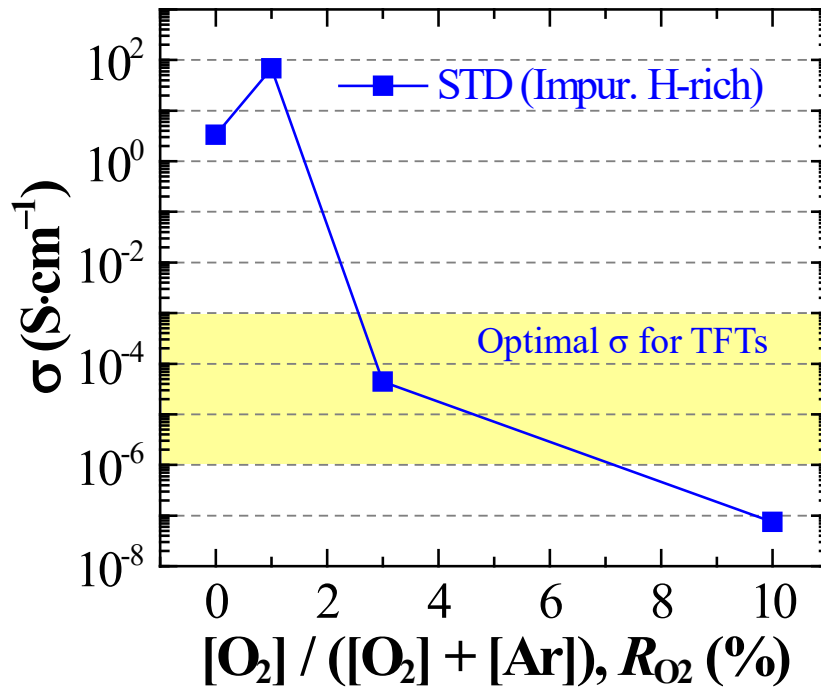
Transfer characteristics
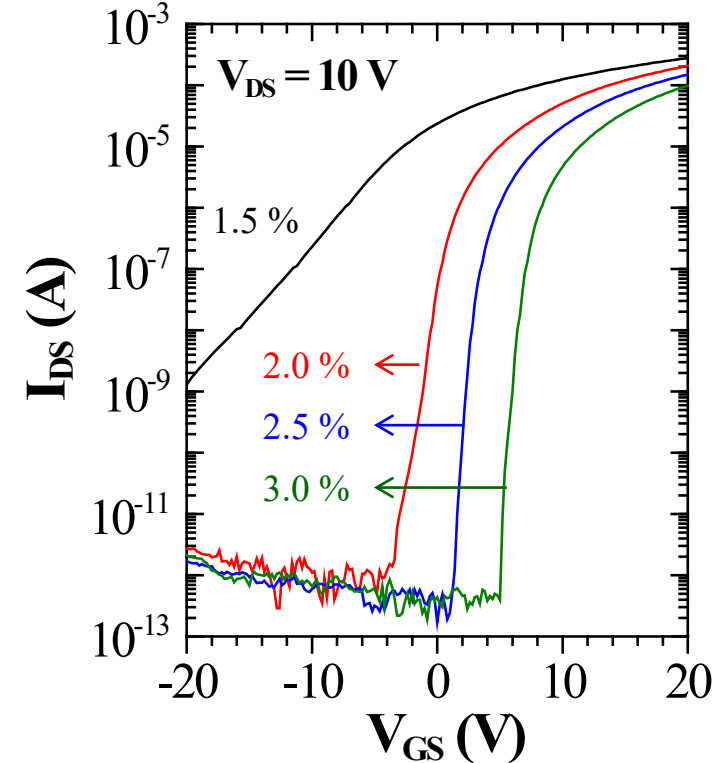
- **Wide window of electrical properties by controlling R_{O2}**
- **Optimal σ for TFT: $10^{-3}-10^{-6}$ S·cm⁻¹ ⇒ R_{O2} = 2−4 %**

Optimum R_{O2} for UHV sputtering?

■ Conductivity: STD vs UHV
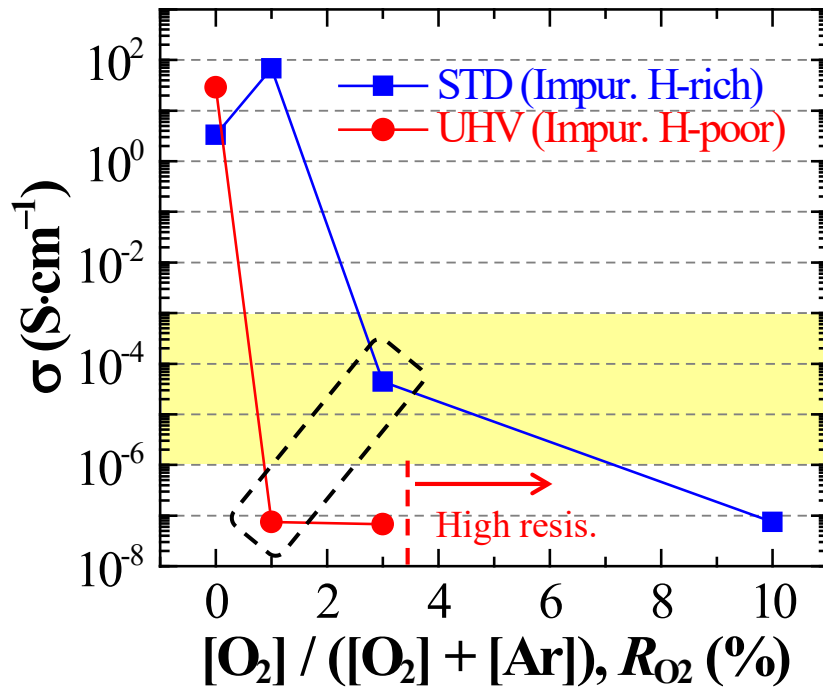
■ Transfer characteristics
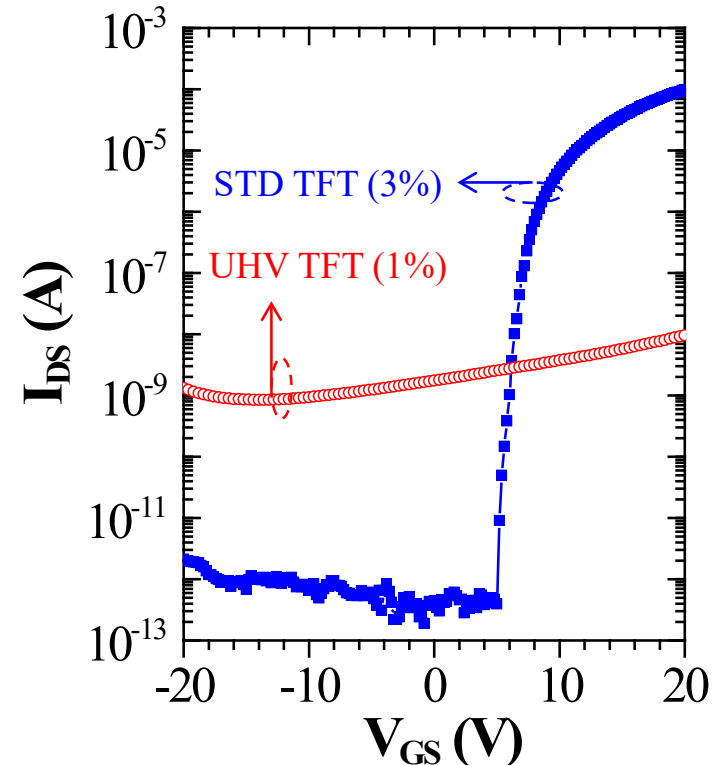
High resistivity UHV a-IGZO films obtained

even if deposited at $R_{O2} = 1 \%$ (RT)

⇒ Further reducing R_{O2} for UHV films?

Very small O₂ is enough for UHV sputt.

Conductivity
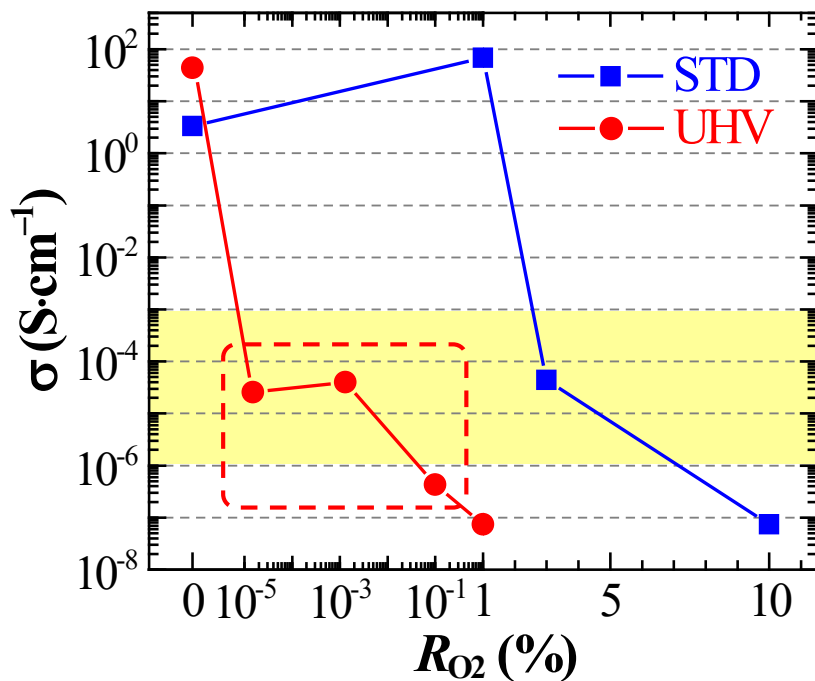
Transfer characteristics
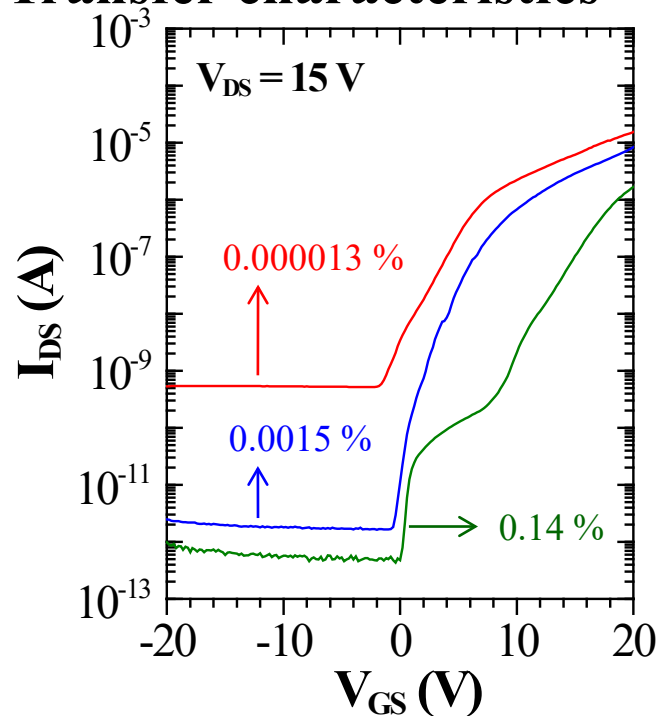
Optimum σ ($10^{-3}-10^{-6}$ S·cm^{-1}) obtained at $R_{O2} = 10^{-5}-10^{-3}$ %

STD films: Extra $R_{O2} = 2-3$ % are required due to impurity H ([H] = 10^{20-21} cm^{-3})

[H] is compensated by P_{O_2}: Is it good?
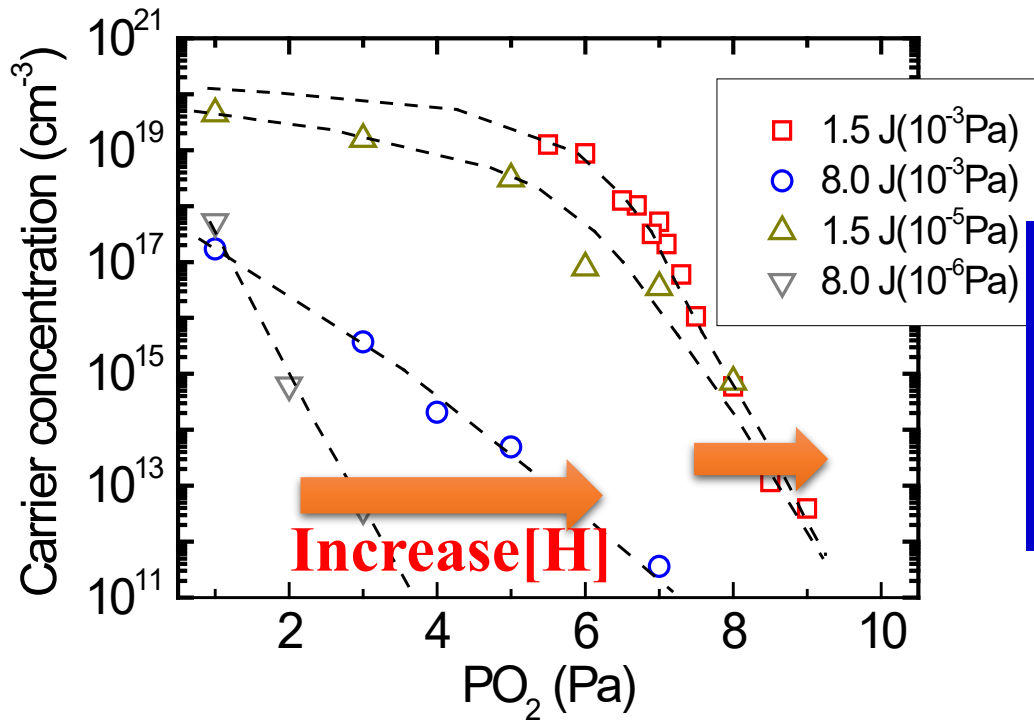
Back pressure ↓
[H] ↑
More O_2 is introduced

Increase[H]

Optimum P_{O_2}
Conventional sputter: ~3 %
Dirty chamber   : larger (>10%?)
Clean chamber   : smaller (down to 10^{-5} %)

Extra instability by H as $\Delta V_{th} \propto t^{1/4}$

Constant V_{GS} stress test
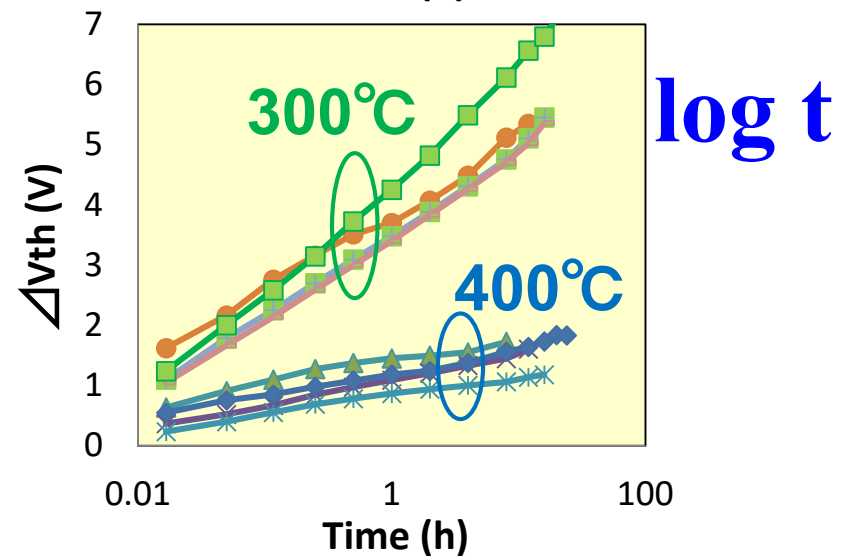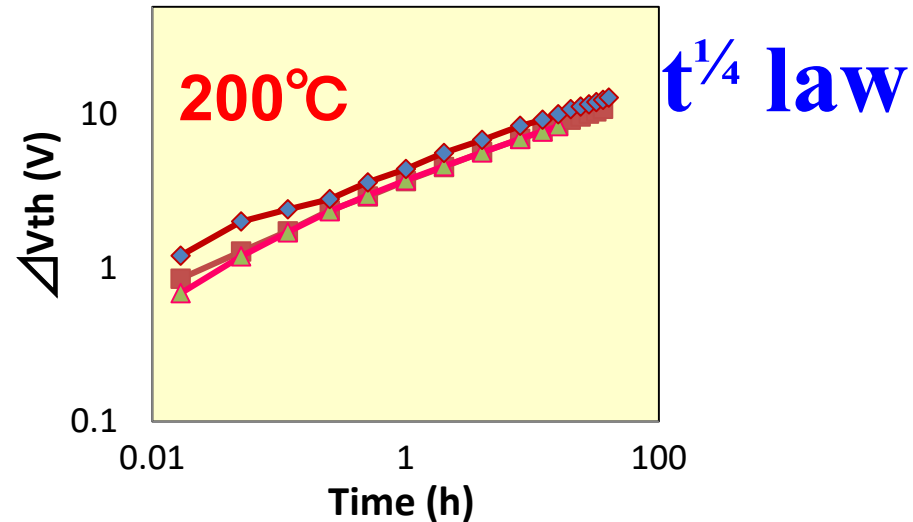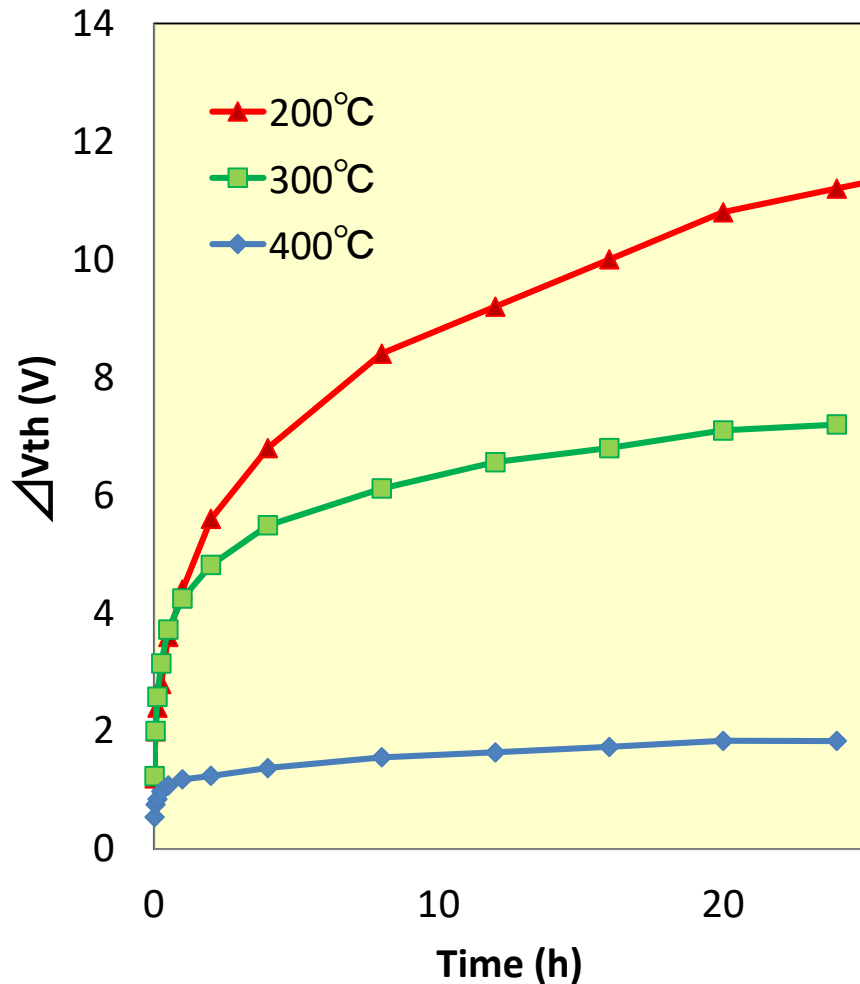
Hydrogen and oxygen in a-IGZO

- **O diffusion ~ 20 nm @ 400°C for 30 minutes**
- **Weakly-bonded O forms bistable trap**
- **Device-quality a-IGZO: $10^{20} - 10^{21}$ cm^{-3} of H, but N_e is low**
- **Hydrogens exist as $-O^{2-}H^+$**

  Free e^- are compensated by excess O

Hydrogen annealing
- **High-T (H$_2$ annealing)**

  Remove O to reduce a-IGZO
- **RT – High T**

  Produce free e^- by desorption as H$_2$O

  * Reduction of [H] & Increase in N$_e$
- **RT – 200°C? (H plasma, H$^+$ implantation)**

  H diffusion >> 100 nm@200°C (c.f. 20 nm for O$_2$@400°C)

  H doping to form –OH, producing free e^-

  M-**O**-M + **H** → M-($O^{2-}H^+$)-M + e^-

CONTENTS as Summary

Part I: General transistors

1. Types of transistors: FET, TFT, SETT

Part II: General FETs / TFTs

2. FETs / TFTs: Structures, Materials, Fabrication

3. FETs / TFTs: Fundamental and evaluations

4. FETs/TFTs: Applications, Requirements

Part III:
Amorphous Oxide Secmicondutor TFTs

END

History of TFT

1950   1960   1970   1980   1990   2000   2010

1948
W. Shockley

1951
pn JFET

1960
Si MOSFET

High-Tc cuprate superconductors
Oxide electronics (ZnO)
Amorphous oxide conductor
Oxide TFT revival

1975 a-Si:H
1979 a-Si:H TFT
Commercialization
1983 5" B/W LCD
1985 10" Color LCD

1961 CdS TFT

1996 Epi-SnO$_2$:Sb
(μ_{eff} ~1 cm^2/Vs)

~1964
poly-SnO$_2$ FET
poly-In$_2$O$_3$ FET (g_m=0.3mhos)
1968 ZnO FET
(g_m=10mhos)

2003 poly-ZnO TFT rush
2005 LCD panel (Casio)
2006 AMOLED panel (ETRI)

1995 AOS

2004/11 AOS TFT

2005/12 Flexible B/W E-Paper
2006/12 Color E-Paper
AMOLED panel (LG)
2007/8 AMOLED panel (Samsung)
Flexible OLED(LG)
2008/1 AMLCD panel (Samsung)
2010 70" 3D LCD (Samsung)
2012 55" AMOLED (LGD)

Disadvantages of a-IGZO

1. **Sensitive to atmospheric molecules**
   O_2, H_2O, H_2
   Important origin of electrical instability
   => **Need gas-tight passivation layer for bottom-gate TFT**

2. **Hysteresis and instability of unannealed TFT**
   => **Thermal annealing**

3. **Large photoresponse**
   even for subgap photons (down to ~2.3 eV)

4. Difficulty in selective etching / dry etching

5. Absence of p-channel operation

Properties of a-InGaZnO$_4$

- **Hall mobility ~ TFT mobility**   **up to ~20 cm^2/Vs**
- **Donor level**   **0.11 eV@N$_D$=9×10^{15} cm^{-3}**

  T. Kamiya et al., J. Displ. Technol. 5, 462 (2009).

- **Dielectric constant**   **ε(DC) ~ 13ε$_0$**

  D.H. Lee et al., EDL, 32, 1695 (2011).

- **Effective mass**   **~ 0.35 m$_e$**

  A. Takagi, Thin Solid Films 486, 38 (2005).

- **Momentum relaxation time**   **up to 5 fs**
- **Mean free path**   **up to 1.0 nm**

  T. Kamiya et al., Appl. Phys. Lett. 96, 122103 (2010).

- **Work function**   **~4.5 eV (4.8 – 5.0 eV for oxidized a-IGZO)**

  Shimura, TSF **516**, 5899 (2008); Hsieh APL **92**, 133503 (2008)
  Lee SSL **1**, Q8 (2012); Lee JAP **112**, 033713 (2012;

- **Thermal diffusivity**   **5.4×10^{-7} m^2/s**
- **Thermal conductivity**   **1.4 W/(m·K)**

  T. Yoshikawa, Appl. Phys. Exp. 6, 021101 (2013).

- **(not Dense) Random Packing Structure**
  Density ~ 5% lower than crystalline InGaZnO$_4$ (6.36 g/cm^3 for c-InGaZnO$_4$)

  K. Nomura et al., Phys. Rev. B 75, 035212 (2007).
  [1] *K. Ide et al., J. Appl. Phys. 111, 073513 (2012).*

- **Crystallization T** [1]   **600°C (sputtered), 700°C (PLD)**

Back End-Of-Line (BEOL) Transistor

Renesas Electronics

IGZO TFT operates at 1.5 – 100 V

Bridge low-V ULSI to high-V circuits/loads

A Novel BEOL Transistor (BETr) with InGaZnO Embedded in Cu-Interconnects for On-chip High Voltage I/Os in Standard CMOS LSIs
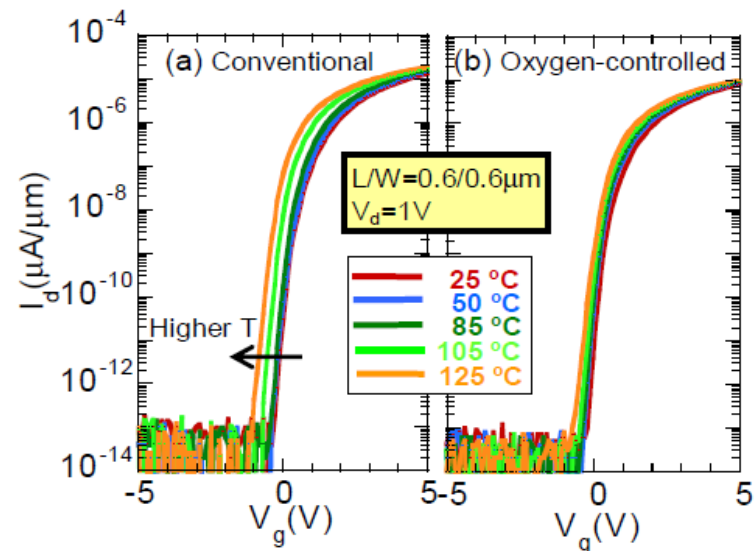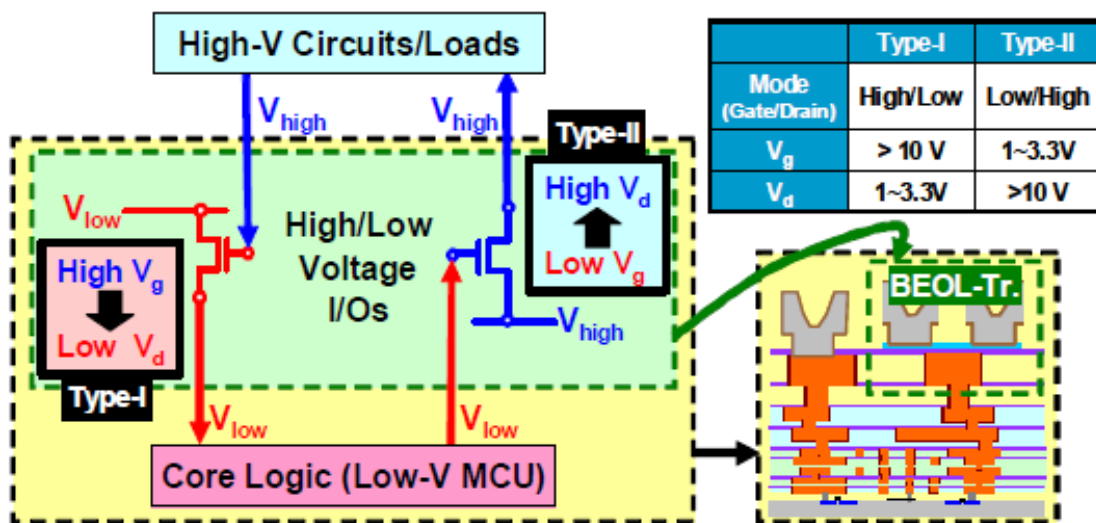
Kishou Kaneko, Naoya Inoue, Shinobu Saito, Naoya Furutake, and Yoshihiro Hayashi

2011 VLSI Symp. (2011) 120

Highly Reliable BEOL-Transistor with Oxygen-controlled InGaZnO and Gate/Drain Offset Design for High/Low Voltage Bridging I/O Operations

K. Kaneko, N. Inoue, S. Saito, N. Furutake, H. Sunamura, J. Kawahara, M. Hane and Y. Hayashi

IEDM2011 (2011) 7.4.1

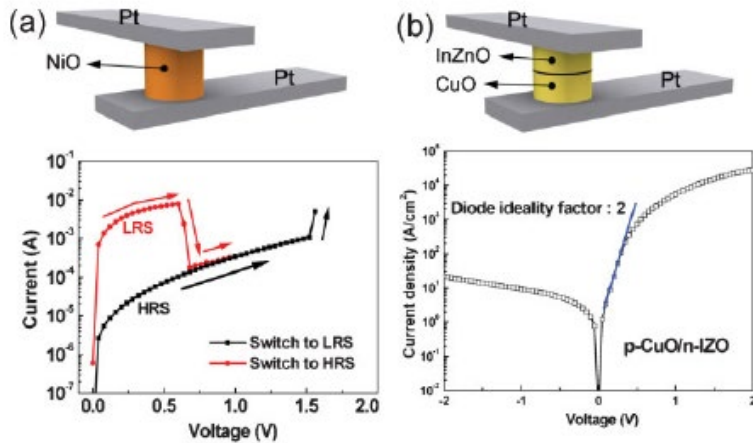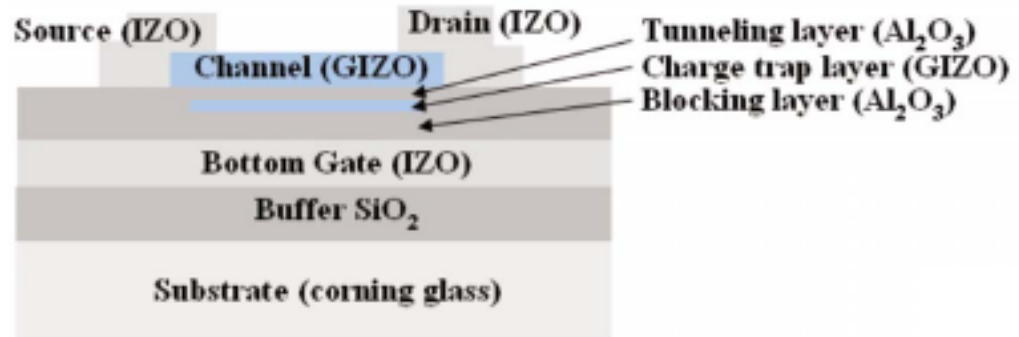# Oxide Non-Volatile Memories

NiO ReRAM memory

*Lee et al., Adv. Mater. **19**, 1587 (2009)*

1Diode + 1Resistor

a-IGZO floating gate memory

*Yin et al, APL **93**, 172109 (2008)*

FeTFT

*Haga et al., Jpn. J. Appl. Phys. **53**, 111103 (2014)*

BLT: $(Bi.,La)_4T_{i3}O_{12}$
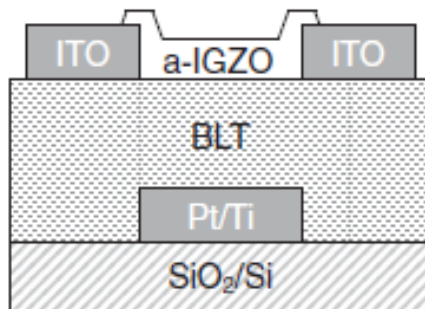
Mixed ion electron ReRAM

Aoki et al., Nat. Comm. 5, 3473 (2014)

a-GaOx
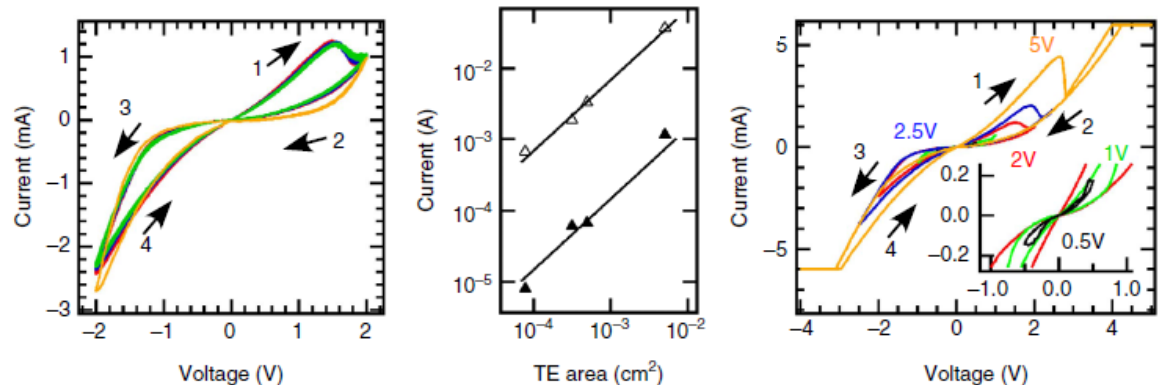
Low-Voltage Operating a-IGZO TFT

T. Kawamura, H. Uchiyama, S. Saito, H. Wakana, T. Mine, M. Hatano, K. Torii and T. Onai

TFTs with a small subthreshold slope (SS) are required for low-voltage operating circuits on large and flexible substrates. Using In-Ga-Zn-O deposited at room temperature for a channel layer, we achieved 63 mV/dec, the smallest SS ever reported for oxide TFTs. To achieve the small SS, a fully-depleted off-state was employed by thinning the channel layer to 6 nm.
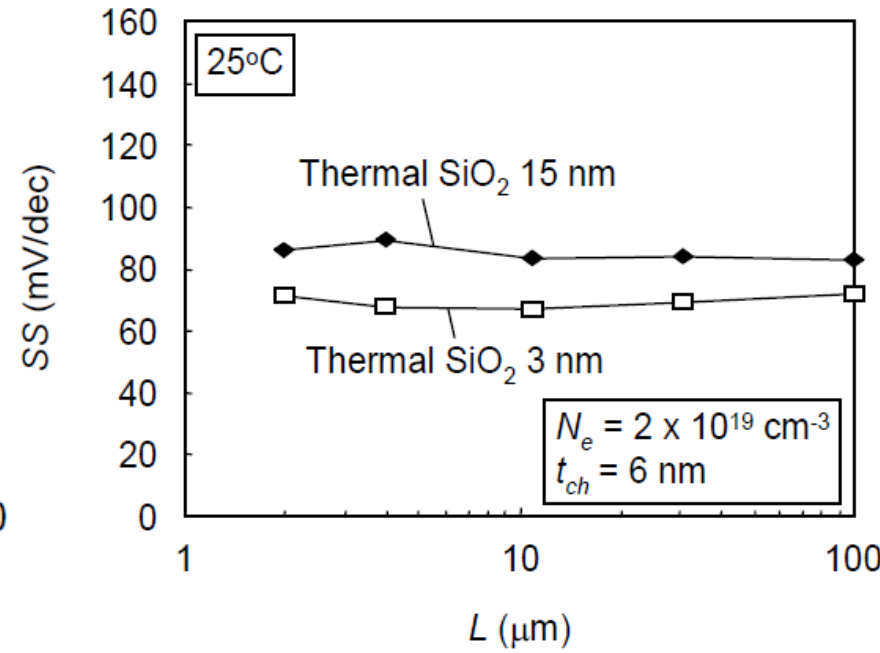
Wireless operations for 13.56-MHz band RFID tag using amorphous oxide TFTs

Hiroaki Ozaki, Tetsufumi Kawamura, Hironori Wakana,
Takanori Yamazoe, and Hiroyuki Uchiyama
IEICE Electronics Express, Vol. 8, No. 4, 225-231

25nm IGZO / SiO$_x$ 100 nm / Mo 70 nm

Mobility 15 cm^2/Vs

Active load inverters

RFID (13.56 MHz): 70mm distance, 5V/40mW input

I$_{dd}$ < 1 nA

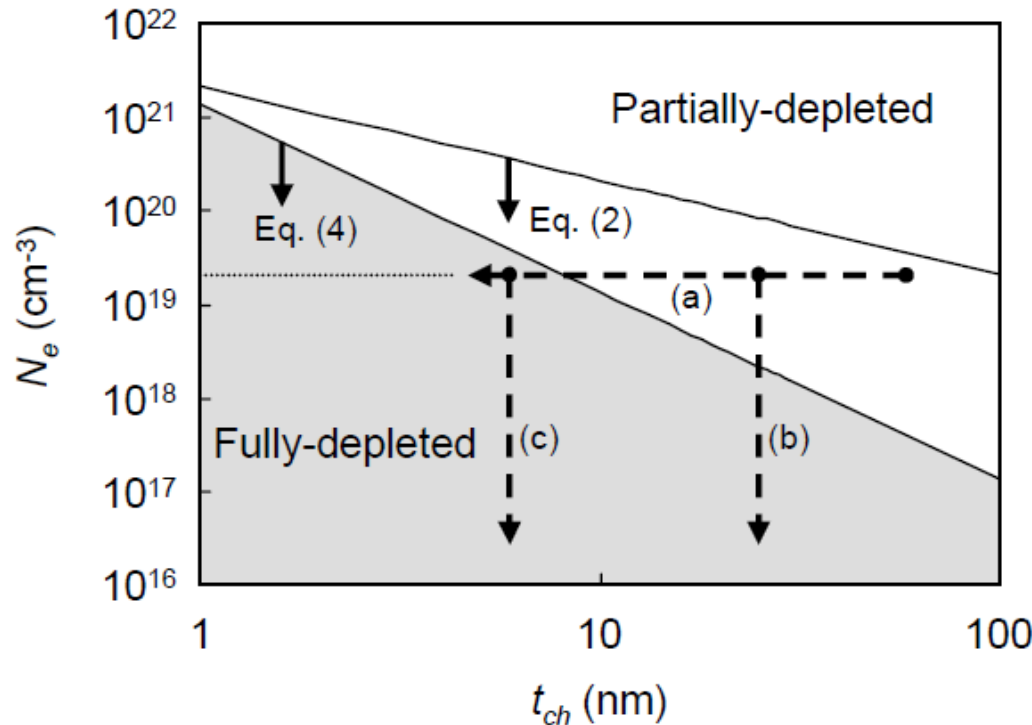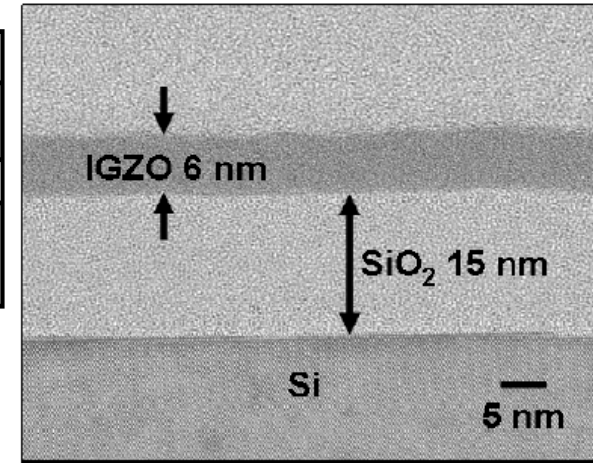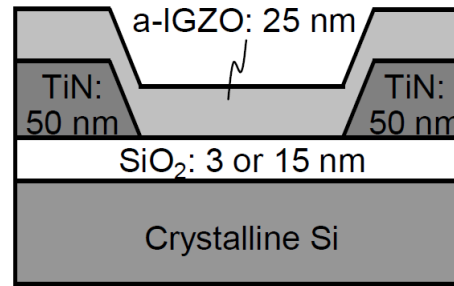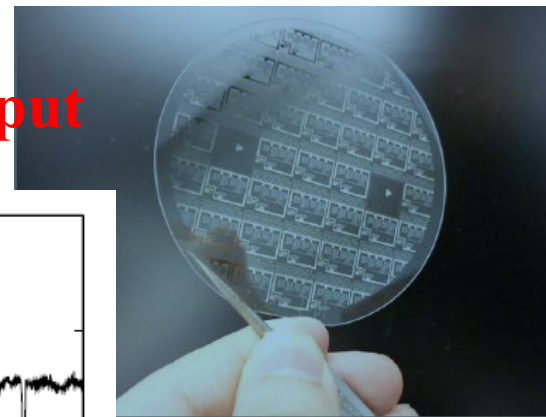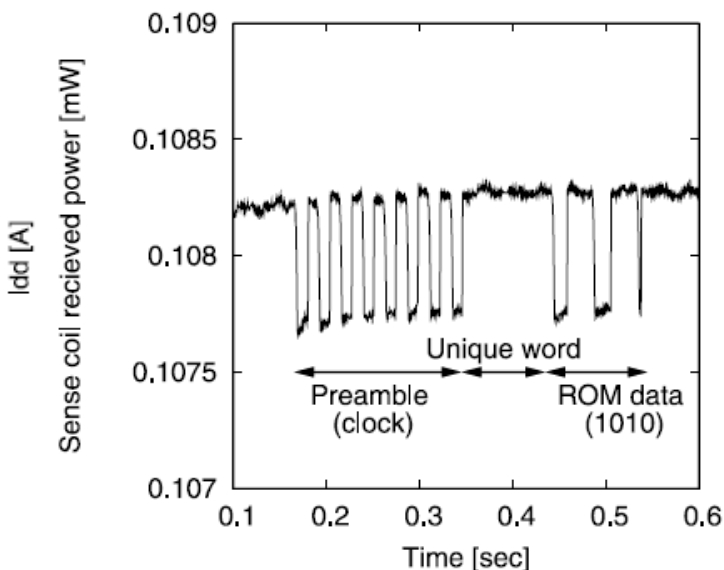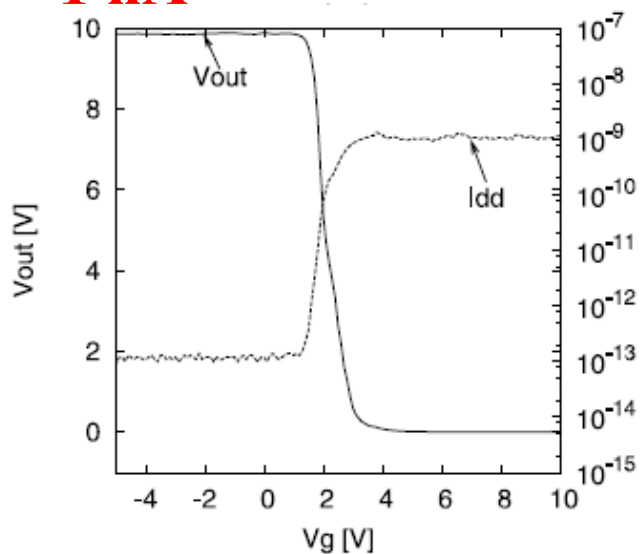Refs. T. Kawamura, H. Uchiyama, S. Saito, H. Wakana, T. Mine, M. Hatano, K. Torii, and T. Onai,
"1.5-V operating fuly-depleted amorphous oxide thin film transistors achieved by 63-mV/dec
subthreshold slope," IEDM Tech. Dig., pp. 77-80, 2008
T. Kawamura, H. Wakana, K. Fujii, H. Ozaki, K. Watanabe, T. Yam wireless operation with DC output
up 12 V," IEDM Tech. Dig., pp. 140-141, Feb. 2010

Roles of In, Ga, and Zn

- **Increasing In, Zn: Mobility increases**
  - **In 5s with O 2p: Main electron transport path**
  - **Zn, Ga: Contribute to electron transport**
- **Increasing Ga: Suppress residual carriers**
  - **Suppress off current**
  - **Increase subthreshold voltage swing?**
- **Multi component system: Form stable amorphous phase**

Controllability of carrier concentration in a-IZO and a-IGZO films

N_e vs. P_{O2}
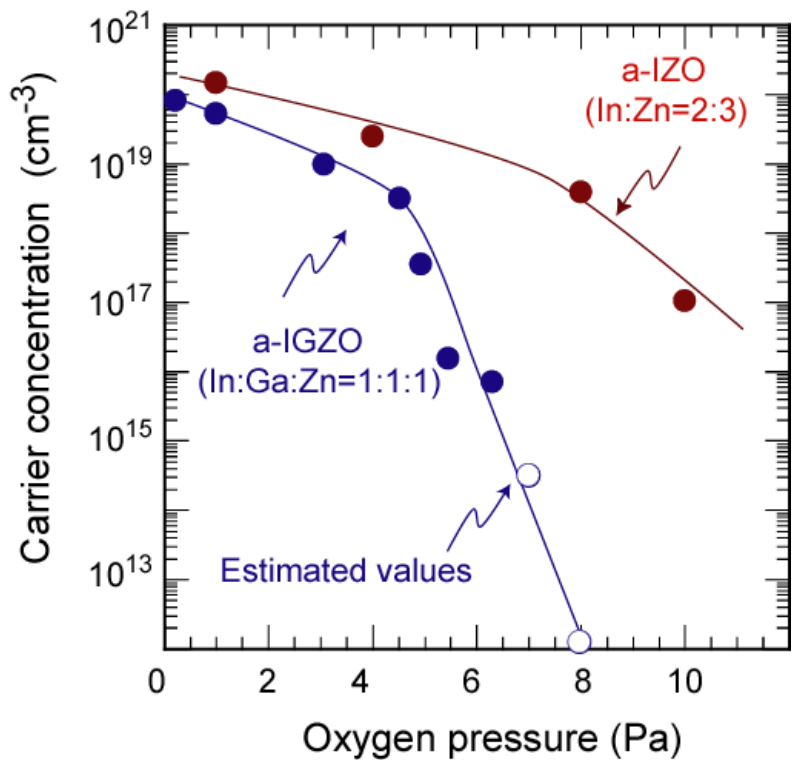
I-V characteristics
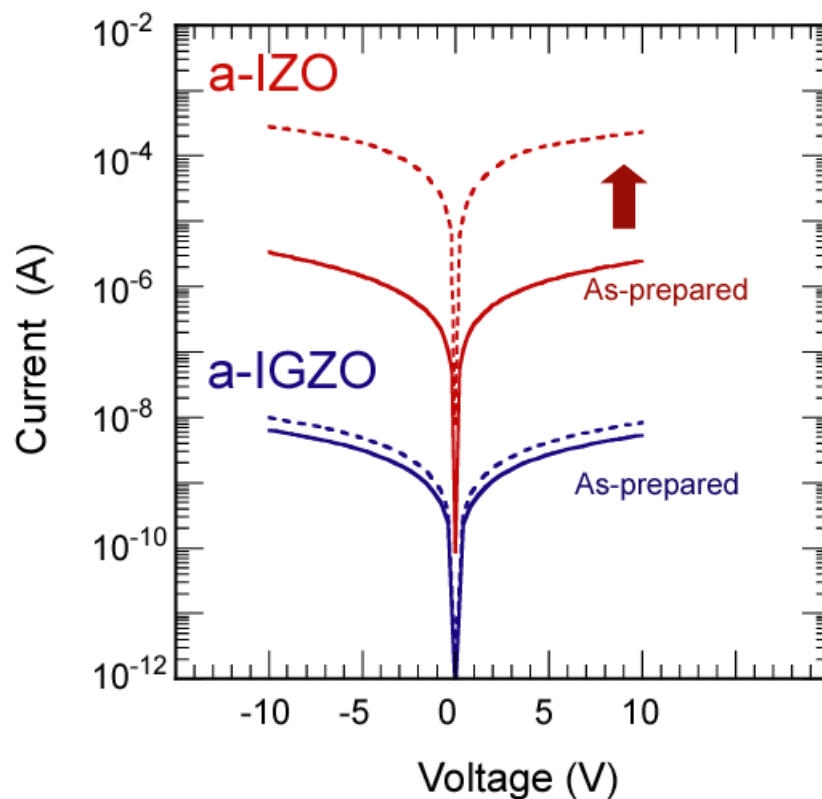
K. Nomura et al.,
Jpn. J. Appl. Phys. **45**, 4303 (2006)

Unusual electron transport
$\mu - N_e$ relation and non-Arrhenius behavior
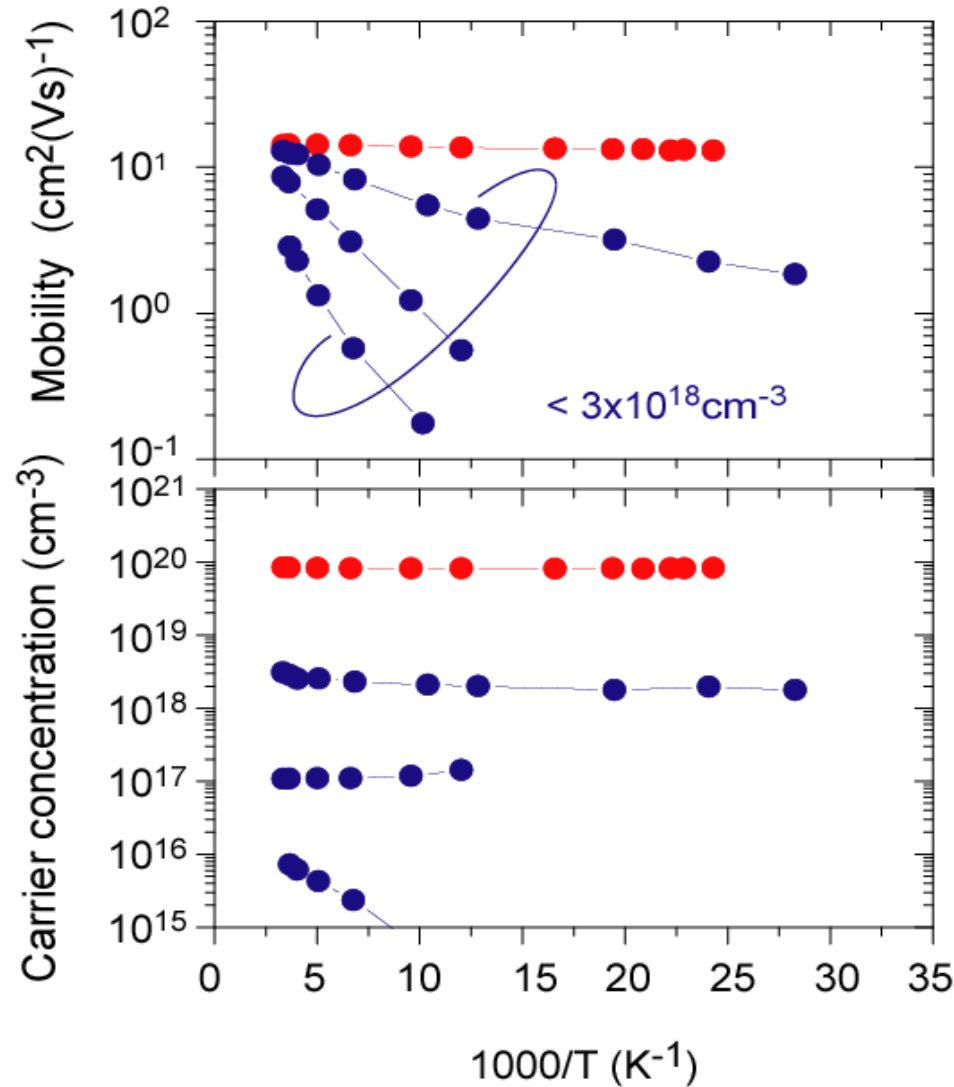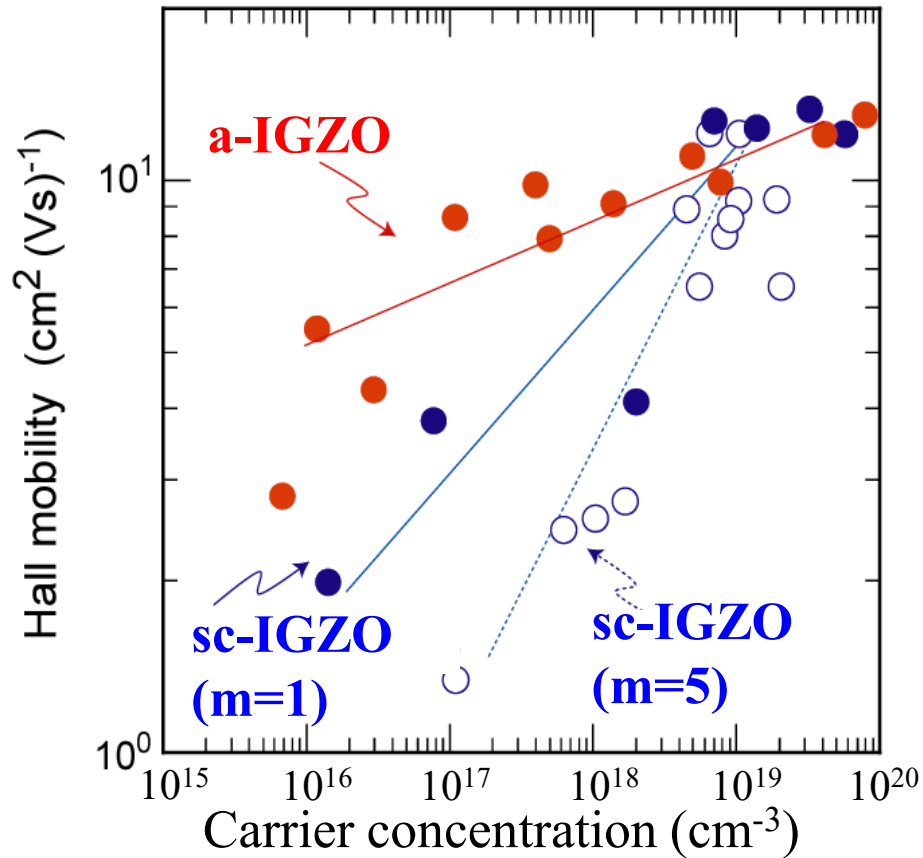
Hall mobility

Sputtered a-IGZO films

Private communication with Dr. Yabuta of Canon
Abe et. al., TSF **520** (2012) 3791

PLD a-IGZO films

Nomura et. al., Nature **432** (2004) 488
Orui et al., JDT **11**, 518 (2014)

μ_{Hall} **up to 20 cm^2/(Vs)**

μ_{Hall} **up to 12 cm^2/(Vs)**

$\mu_{Hall} \propto (N_e)^{\gamma/2}$

c-IGZO5

c-IGZO1

LQ P$_{base}$ a-IGZO

HQ a-IGZO

LQ a-IGZO
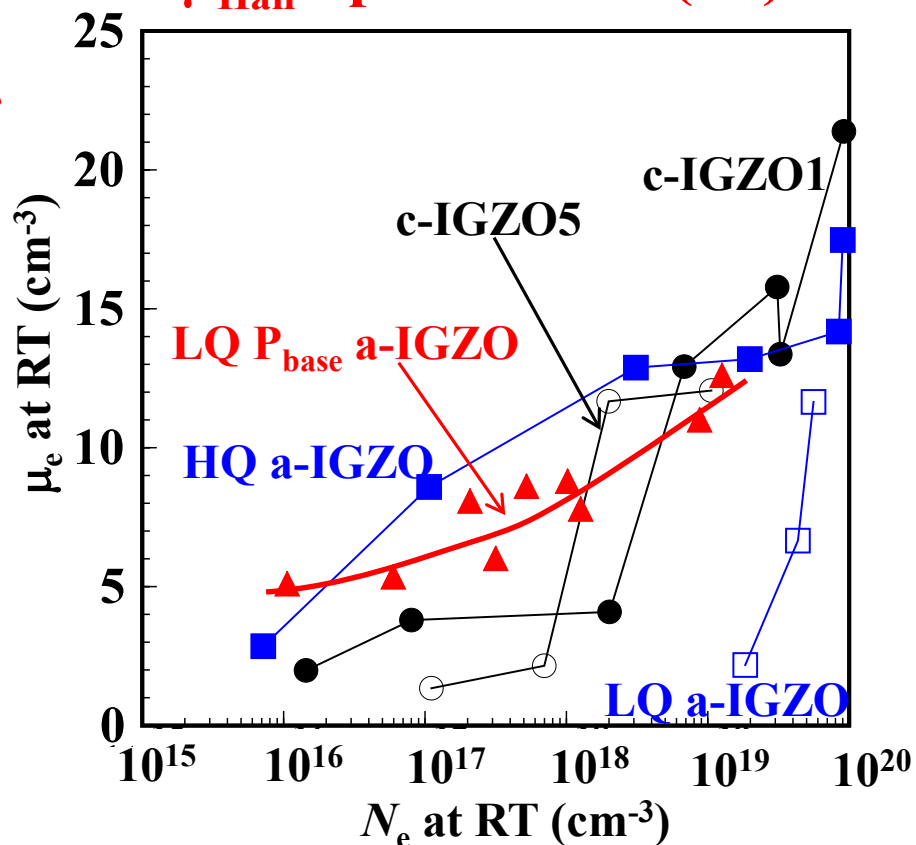
Wet processes

IZO: In-Zn-O,   IGZO: In-Ga-Zn-O,ZTO: Zn-Sn-O, IGO: In-Ga-O, IZTO: In-Zn-Sn-O,AITO: Al-In-Sn-O, ZITO: Zn-In-Sn-O,

HIZO: Hf-In-Zn-O, SC: Spin coat, IJ: Ink-jet, PC SG: Photo-chemical sol-gel

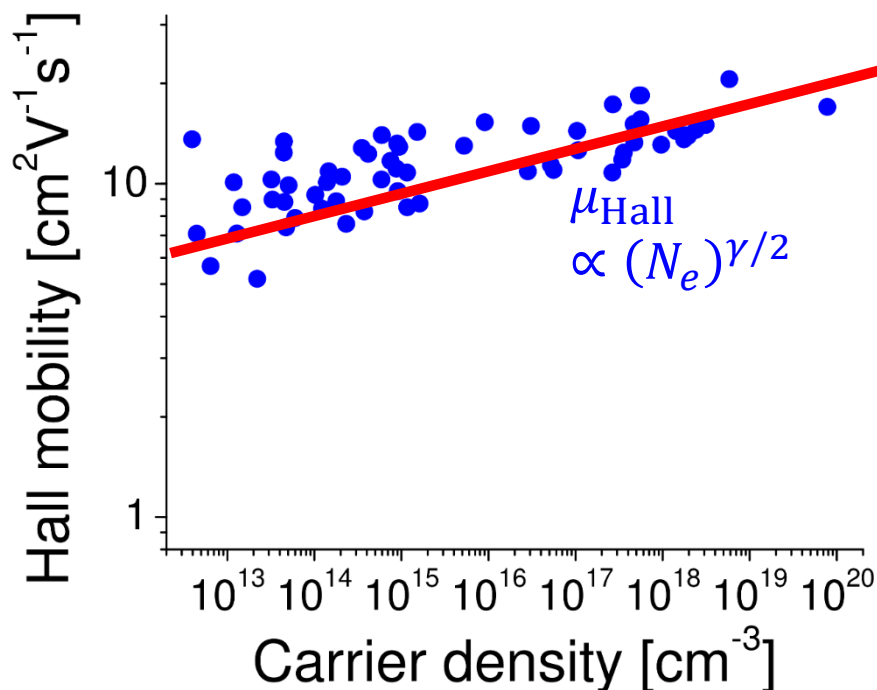| Material	Mobility (cm^2/Vs)	Method	Solution	T (^{o}C)	Ref.
a-IZO	16.1	SC	$ZnCl_2$, $InCl_3$	600	D.-H. Lee et al., Adv. Mater. 19, 843 (2007)
a-IZO	7.4	IJ	$ZnCl_2$, $InCl_3$	600	D.-H. Lee et al., Adv. Mater. 19, 843 (2007)
a-IZO	7.3	IJ	$Zn(OAc)_2$, $In(OAc)_3$	500	C.G. Choi et al., Electrochem. Sol. Stat. Lett. 11, H7 (2008)
a-IZO	2.13	SC	$ZnCl_2$, $InCl_3$	500	C.-K. Chen et al., J. Displ. Technol. 5, 509 (2009)
a-IZO	6.6	SC	$Zn(OAc)_2$, $In(OAc)_3$	450	K.-HB Park et al., Electron. Dev. Lett. 31, 311 (2010)
a-IZO	1.54	SC	$Zn(OAc)_2$, $In(OAc)_3$	400	S. Jeong et al., Adv. Mater. 22, 1346 (2010)
IZO	3.3	SC	Commercially available solution	400	S.-M. Yoon et al., Electrochem. Sol.-Stat. Lett. 13, H141 (2010)
a-IZO	5.0	SC		450	M.K. Ryu et al., J. Soc. Inf. Displ. 18, 734 (2010)
IZO	0.54	SC	$Zn(OAc)_2$, $In(OAc)_3$	300	C.Y. Koo et al., J. Electrochem. Soc. 157, J111 (2010)
IGO	9	IJ	$Ga_7In_6(\mu3-OH)_6(\mu-OH)_{18}(H_2O)_{24}(NO_3)_{15}$	600	Z.L. Mensinger et al., Angew. Chem. 47, 9484 (2008)
IGZO	0.96	SC	$Zn(OAc)_2$, $Ga(NO_3)_3$, $In(NO_3)_3$	450	G.H. Kim et al., J Electrochem. Soc. 156, H7 (2009)
IGZO	1.25	SC	$Zn(OAc)_2$, $Ga(NO_3)_3$, $In(NO_3)_3$	400	G.H. Kim et al., Appl. Phys. Lett. 94, 23501 (2009)
a-IGZO	3~16	SC	$Zn(OAc)_2$, $Ga(NO_3)_3$, $In(NO_3)_3$	400	D. Kim et al., Appl. Phys. Lett. 95, 10350 (2009
a-IGZO	0.85	SC	$Zn(OAc)_2$, $Ga(NO_3)_3$, $In(NO_3)_3$	400	S. Jeong et al., Adv. Mater. 22, 1346 (2010)
a-IGZO	0.52	SC	$Zn(OAc)_2$, $Ga(NO_3)_3$, $In(NO_3)_3$	500	Y.-H. Kim et al., IEEE Trans. Electron. Dev. 57, 1009 (2010)
a-IGZO	0.05	IJ	$Zn(OAc)_2$, $Ga(NO_3)_3$, $In(NO_3)_3$	400	D. Kim et al., Jpn. J. Appl. Phys. 49, 05EB06 (2010)
a-IGZO	2.07			450	Y.-C. Lai et al., Proc. IDW'09, 1697 (2009)
a-IGZO	0.86	SC	$Zn(OAc)_2$, $Ga(NO_3)_3$, $In(NO_3)_3$	450	G. Kim et al., Phys. Stat. Sol. (a) 207, 1677 (2010)
IGZO	0.46	SC	$Zn(OAc)_2$, $Ga(NO_3)_3$, $In(NO_3)_3$	550	H.S. Shin et al., Jpn. J. Appl. Phys.. 49, 03CB01 (2010)
IGZO	1.94	SC	$Zn(OAc)_2$, $Ga(NO_3)_3$, $In(NO_3)_3$	500	W.H. Jeong et al, Appl. Phys. Lett. 96, 093503 (2010)
IGZO	2.3	SC	$Zn(OAc)_2$, $Ga(NO_3)_3$, $In(NO_3)_3$	95	Y.-H. Yang et al., IEEE Electron. Dev. Lett. 31, 329 (2010)
a-IGZO	1.3	SC	$Zn(OAc)_2$, $GaCl_2$, $InCl_3$	600	Y. Wang et al., J. Sol.-Gel. Sci. Technol. 55, 322 (2010)
a-IGZO	5.4	SC		270	M. Ito et al., Proc. IMID2010 (2010)
a-IZTO	30	IJ	$InCl_3$, $ZnCl_2$, $SnCl_2$	600	D.-H. Lee et al., J. Mater. Chem. 19, 3135 (2009)
a-ITO	10~20	SC	$InCl_3$, $SnCl_4$	250	H.S. Kim et al., J. Am. Chem. Soc. 131, 10826 (2009)
YIZO	1.92	SC	$Zn(OAc)_2$, $In(NO_3)_3$, $Y(NO_3)_3$	550	H.S. Shin et al., Jpn. J. Appl. Phys. 49, 03CB01 (2010)
AITO	13.3	SC	$In(OAc)_2$, $SnCl_2$, $Al(acac)_3$	500	J.H. Jeon et al., Appl. Phys. Lett. 96, 21209 (2010)
a-ZITO	10~100	SC	$Zn(OAc)_2$, $InCl_3$, $SnCl_2$	400	M.G. Kim et al., J. Am. Chem. Soc. 132, 10352 (2010)
HIZO	1.94	SC	$Zn(OAc)_2$, $HfCl_4$, $In(NO_3)_3$	500	W.H. Jeong et al., Appl. Phys. Lett. 96, 093503 (2010)
IGZO	8.76	PC SG	$In(NO_3)_3$, $Ga(NO_3)_3$, $Zn(CH_3CO_2)_2$	RT	Y.-H. Kim et al., Nature 489, 128 (2012)
IZO	4.43	PC SG	$In(NO_3)_3$, $Ga(NO_3)_3$, $Zn(CH_3CO_2)_2$	RT	Y.-H. Kim et al., Nature 489, 128 (2012)
In_2O_3	11.29	PC SG	$In(NO_3)_3$, $Ga(NO_3)_3$, $Zn(CH_3CO_2)_2$	RT	Y.-H. Kim et al., Nature 489, 128 (2012)

Super widegap AOS possible?
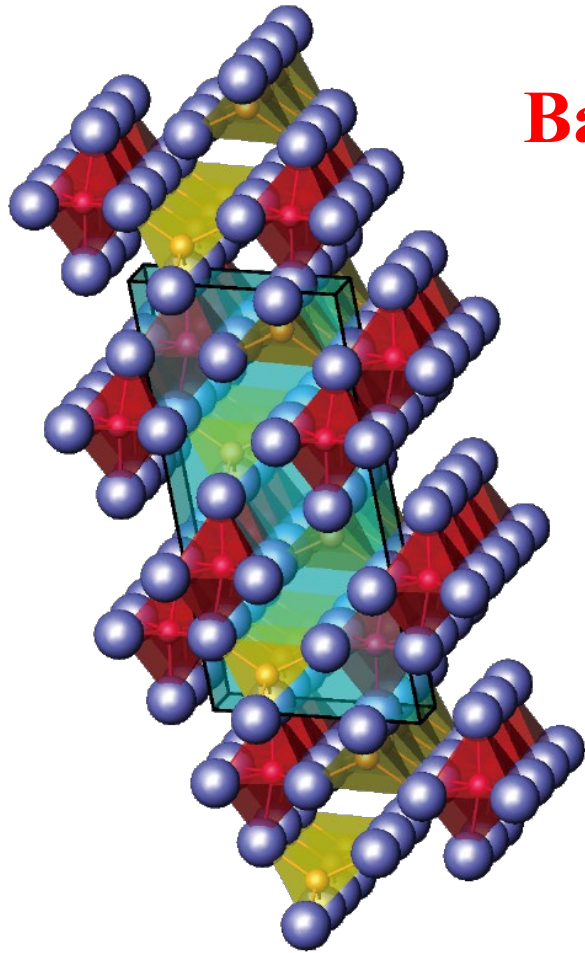
Based on β-Ga$_2$O$_3$:

E_g: 4.9 eV
Transparent to DUV (λ < 300 nm)
Electron doped by Sn, Si etc

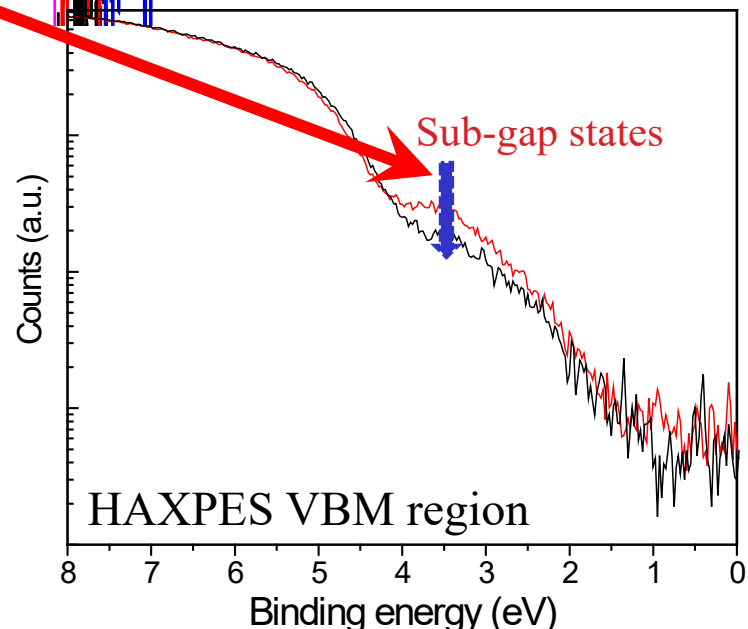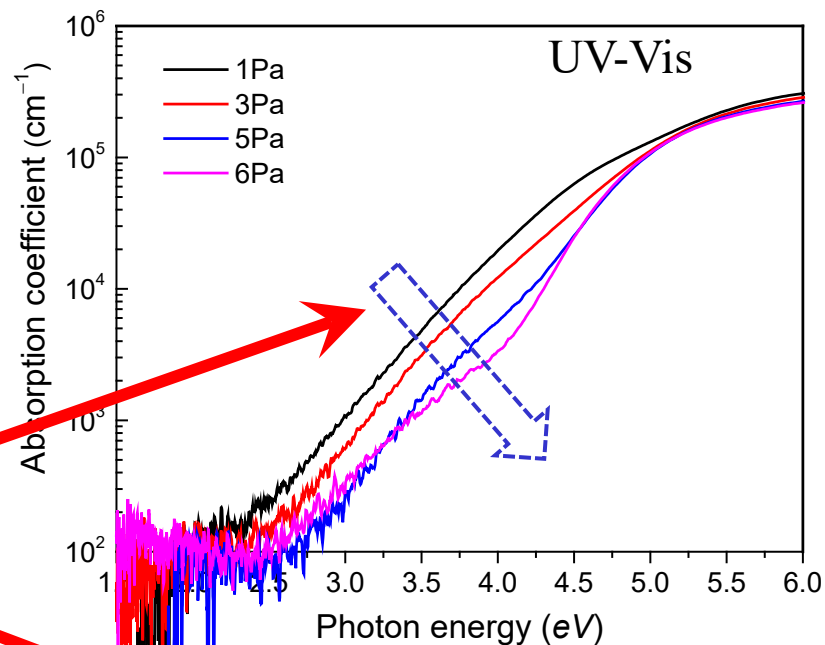**But, never succeeded in producing conducting a-Ga$_2$O$_3$**

Low P_{O2} generates e^- traps
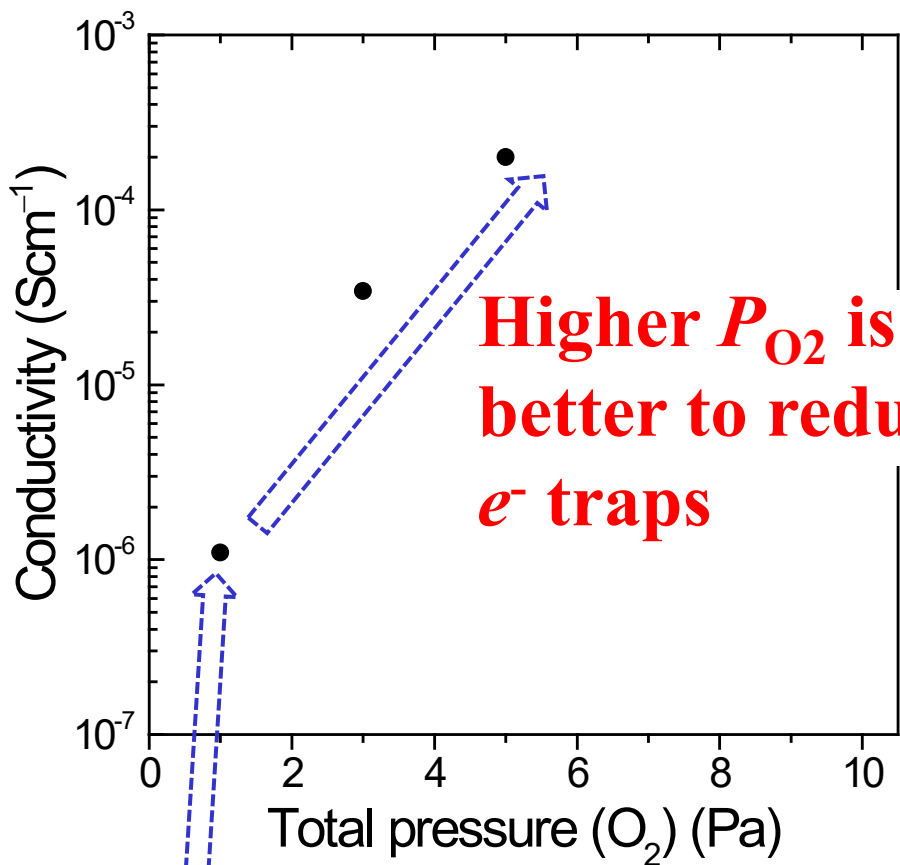
Higher P_{O2} is better to reduce e^- traps

Insulating

UV-Vis

- 1Pa
- 3Pa
- 5Pa
- 6Pa

Sub-gap states

HAXPES VBM region

Density is key to conducting a-Ga$_2$O$_3$
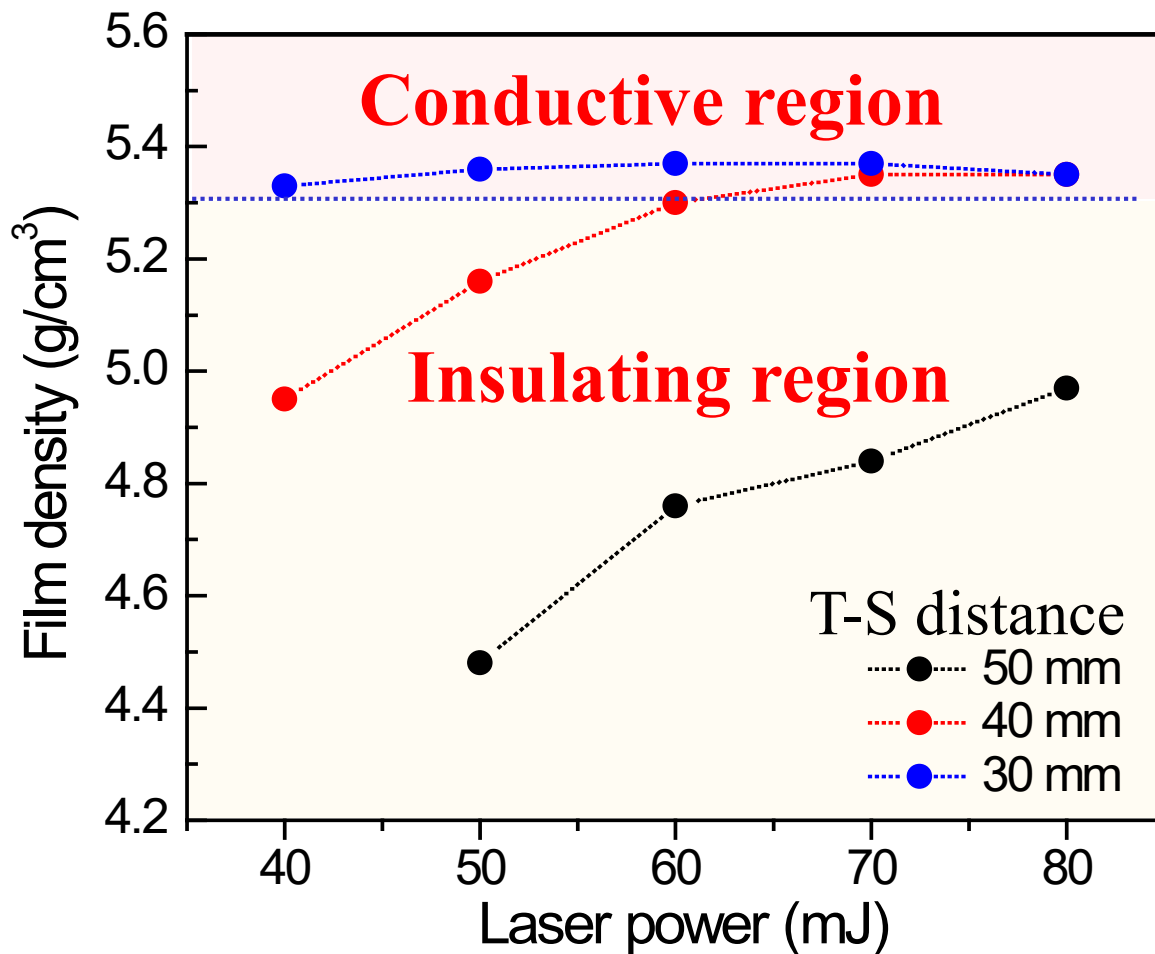
Semiconducting a-Ga$_2$O$_x$ is obtained for film densities > 5.3 g/cm^3

Subgap trap DOSs by different methods

T. Kamiya et al., Sci. Technol. Adv. Mater.. **11** (2010) 044305

a-Si:H

TCAD, annealed
depletion type   (E_u=0.14 eV)
enhancement type (E_u=0.08 eV)
CPM, as-grown (E_u=0.135 eV)
C-V, annealed
(0.013-0.102 eV)

Y-axis: DOS / cm⁻³ /eV

X-axis: E_C - E / eV
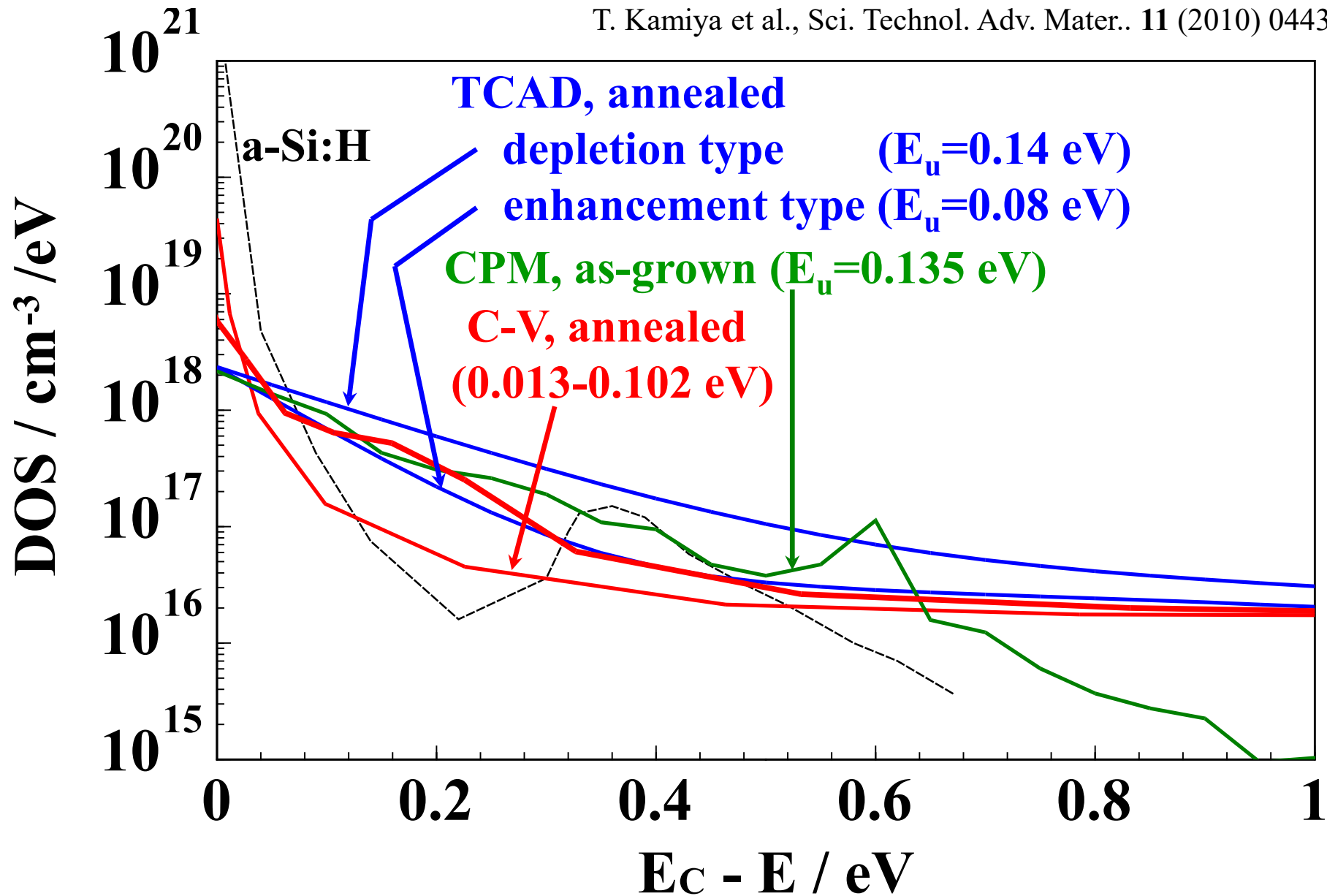
Summary: Subgap DOSs

TCAD, CPM (apparent for near-CB)

- **Overestimation of CB tail states**

    N_e dependence of mobility

    Optical transition from

                near-VBM traps

C-V (real near-CB states)

- **CB tail state width ~ RT (26 meV)**

    No CB tail state?

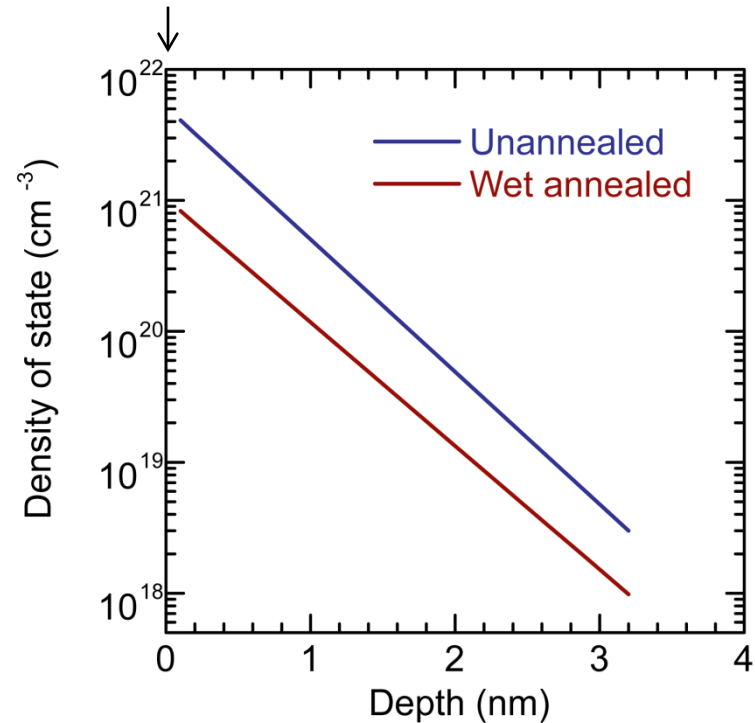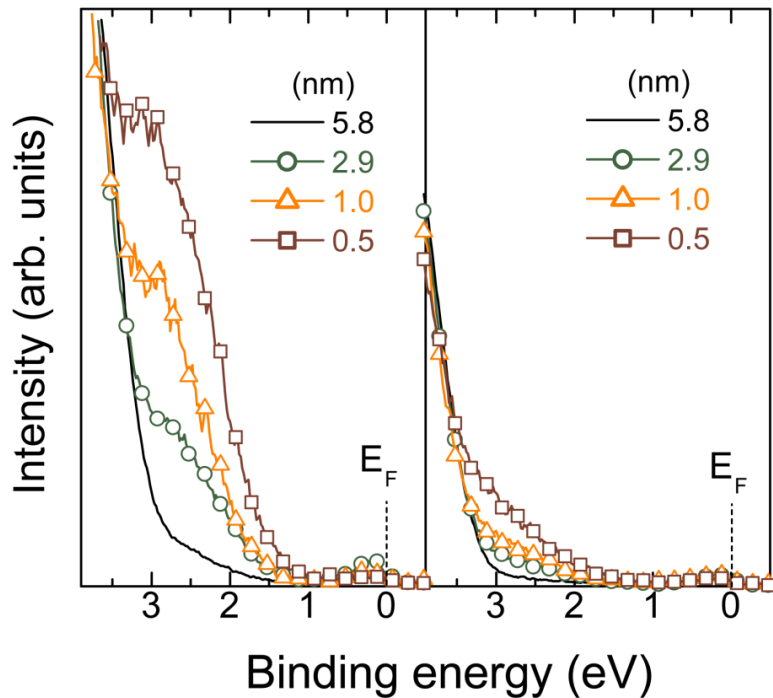- **μ_e – N_e explained by percolation model**

Near-VBM states:
Surface state for PLD HQ a-IGZO

Angle dependent
HX-PES spectra

K. Nomura et al., JAP **109** (2011) 073726

Unannealed **Wet-annealed**
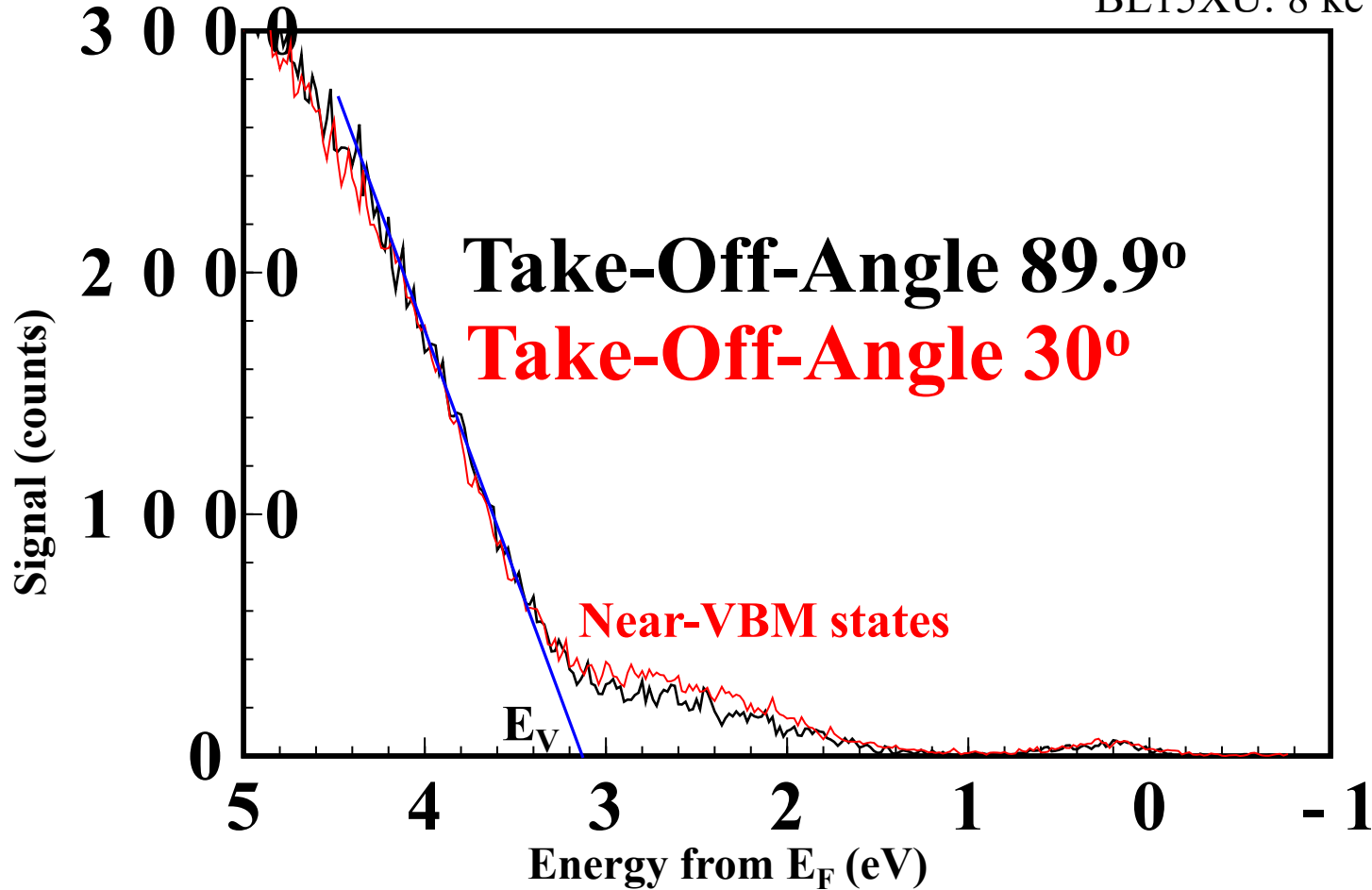
Subgap DOS depth profile
Film surface

Subgap defect
(Peak energy ~2.7eV, width ~1.5eV)

➡ **d < 2nm: 10^{20} cm^{-3}**

Bulk near-VBM states for sputtered a-IGZO

STD sputter, HQ, unannealed a-IGZO

BL15XU: 8 keV HAX-PES

Take-Off-Angle 89.9°
Take-Off-Angle 30°

Near-VBM states

E_V

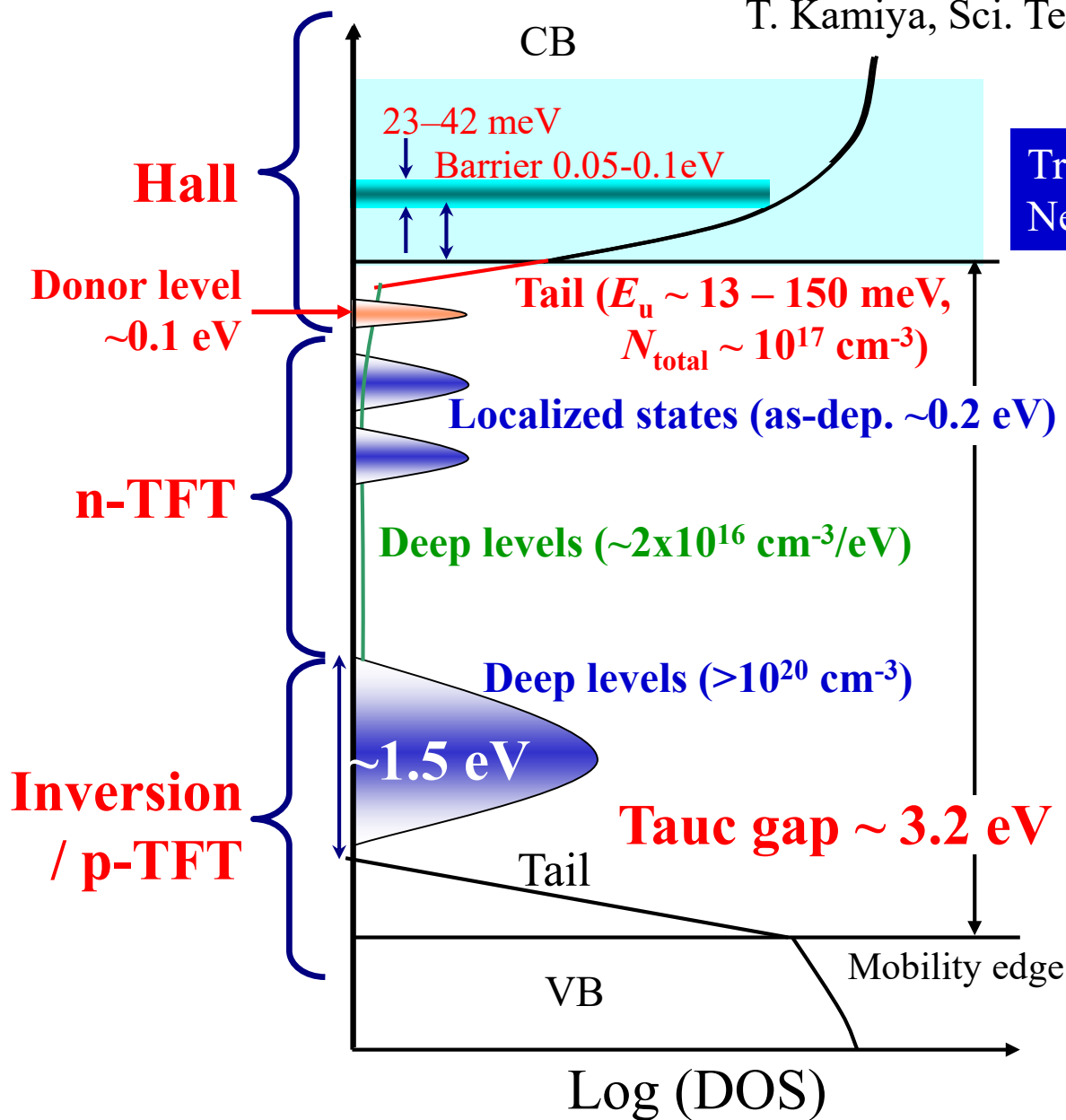Signal (counts)

Energy from E_F (eV)

Near-VBM states: No angle dependence
=> Bulk states at least in ~6 nm surface thickness

Subgap states in a-IGZO

T. Kamiya, Sci. Technol. Adv. Mater, **11**, 044305 (2010)
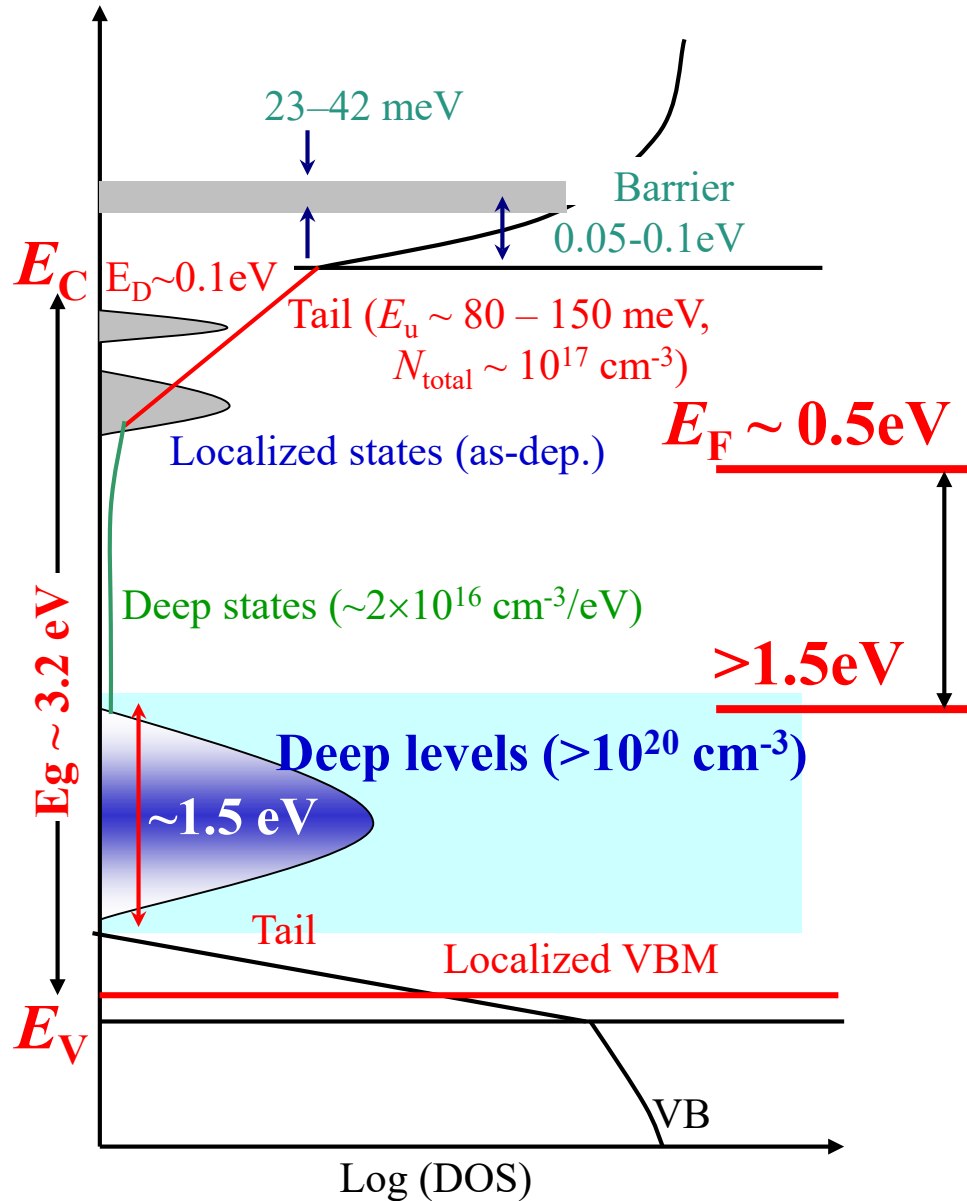Digest of IDW'14, AMD2-1.
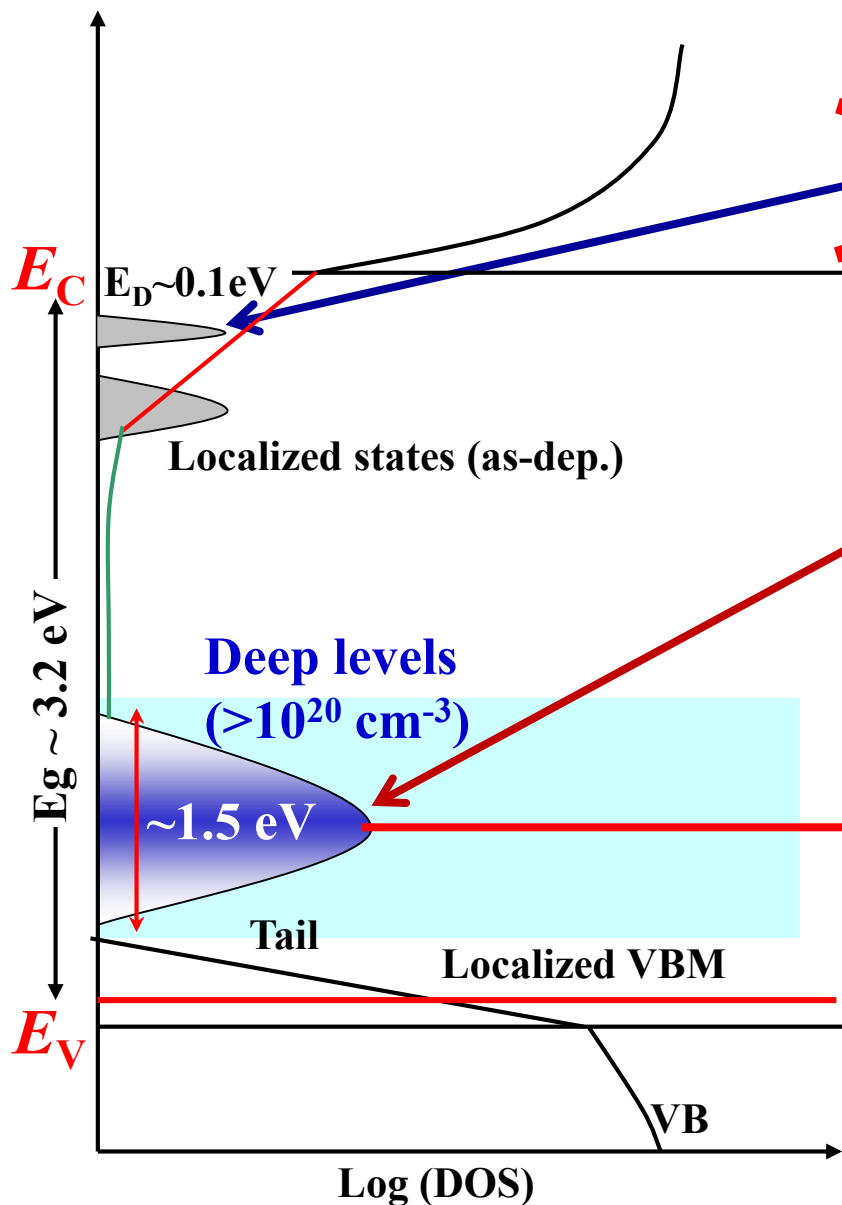
Effects of deep traps

- Low off current
- No p-channel operation
- Subgap photoresponse
- Complex annealing effect
- **Inert for electron transport owing to large bandgap**

Reducing the deep traps will improve …

- **Photoresponse of TFT**
- **Thermal instability**

Figure labels:
23–42 meV
Barrier 0.05-0.1eV
E_C
$E_D \sim 0.1eV$
Tail ($E_u \sim 80 – 150$ meV, $N_{total} \sim 10^{17}$ cm^{-3})
Localized states (as-dep.)
$E_F \sim 0.5eV$
Deep states ($\sim 2 \times 10^{16}$ cm^{-3}/eV)
>1.5eV
Eg ~ 3.2 eV
Deep levels (>10^{20} cm^{-3})
~1.5 eV
Tail
Localized VBM
E_V
VB
Log (DOS)

Origin of negative V$_{th}$ shift by 150-200°C ann.

T. Kamiya, H. Hosono, ECS Trans. **54**, 103 (2013)
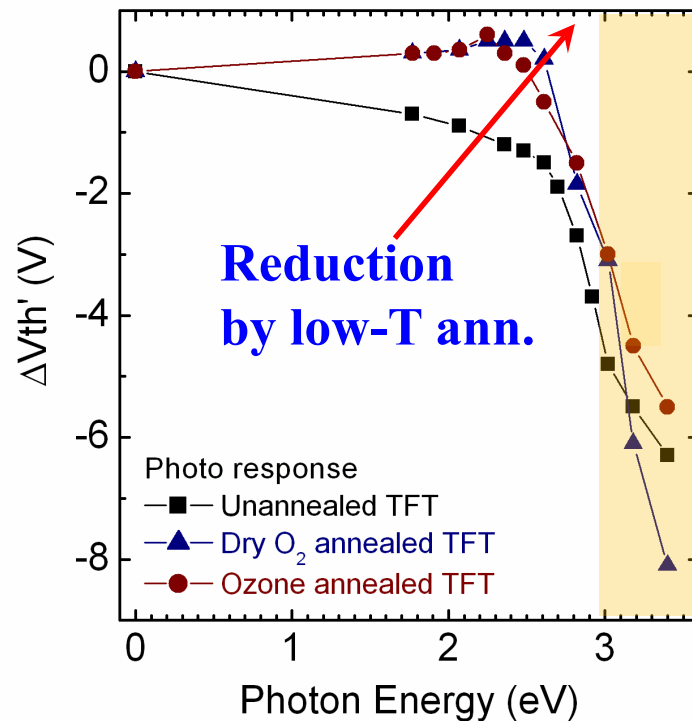
Weakly-bonded oxygen forms deep trap

Hall

Donor level ~0.1 eV

23–42 meV

CB

Barrier ~0.1eV

Tail ($E_u \sim 13 - 150$ meV, $N_{total} \sim 10^{17}$ cm^{-3})

Localized states (as-dep. ~0.2 eV)

n-TFT

Deep levels (~2×10^{16} cm^{-3}/eV)

Deep levels (>10^{20} cm^{-3}) near surface

Vo with void? In$^+$?

Inversion / p-TFT

Tail

Weakly-bonded O^{n-}

Mobility edge

VB

Log (DOS)

Deep trap case: a-IGZO:V_O

T. Kamiya et al., phys. Stat. sol. A **207**, 1698 (2010)

LUMO
V_O
(unoccupied)

V_O
(occupied)

V_O forms both
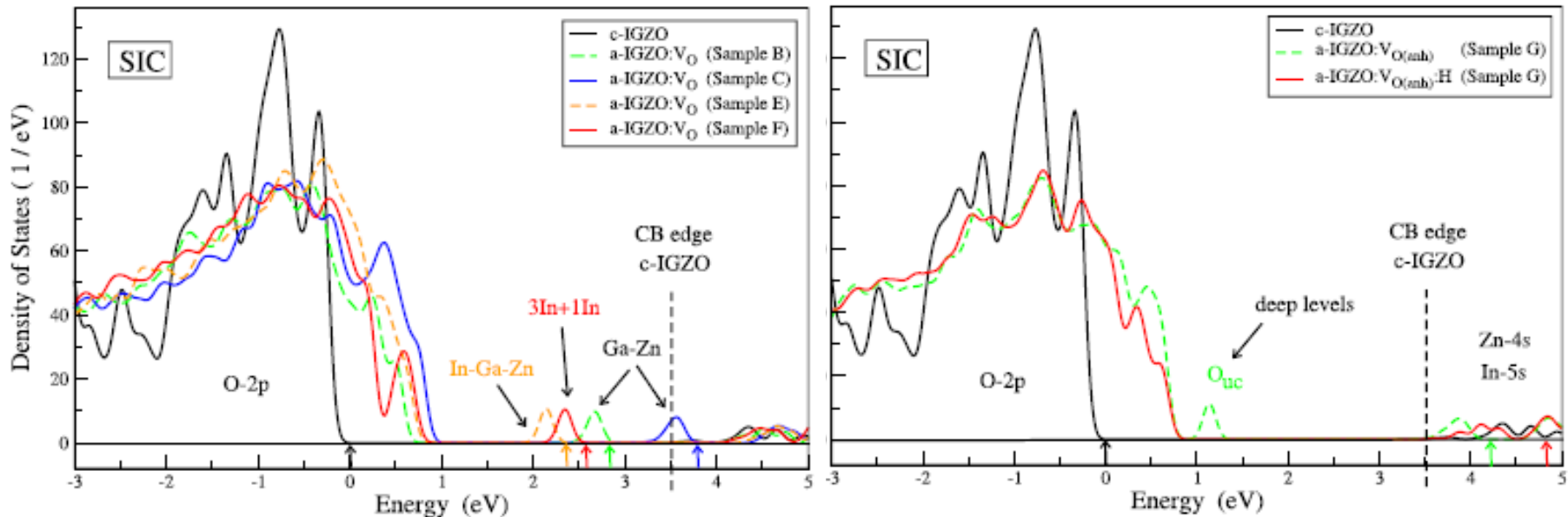a deep state and an electron trap
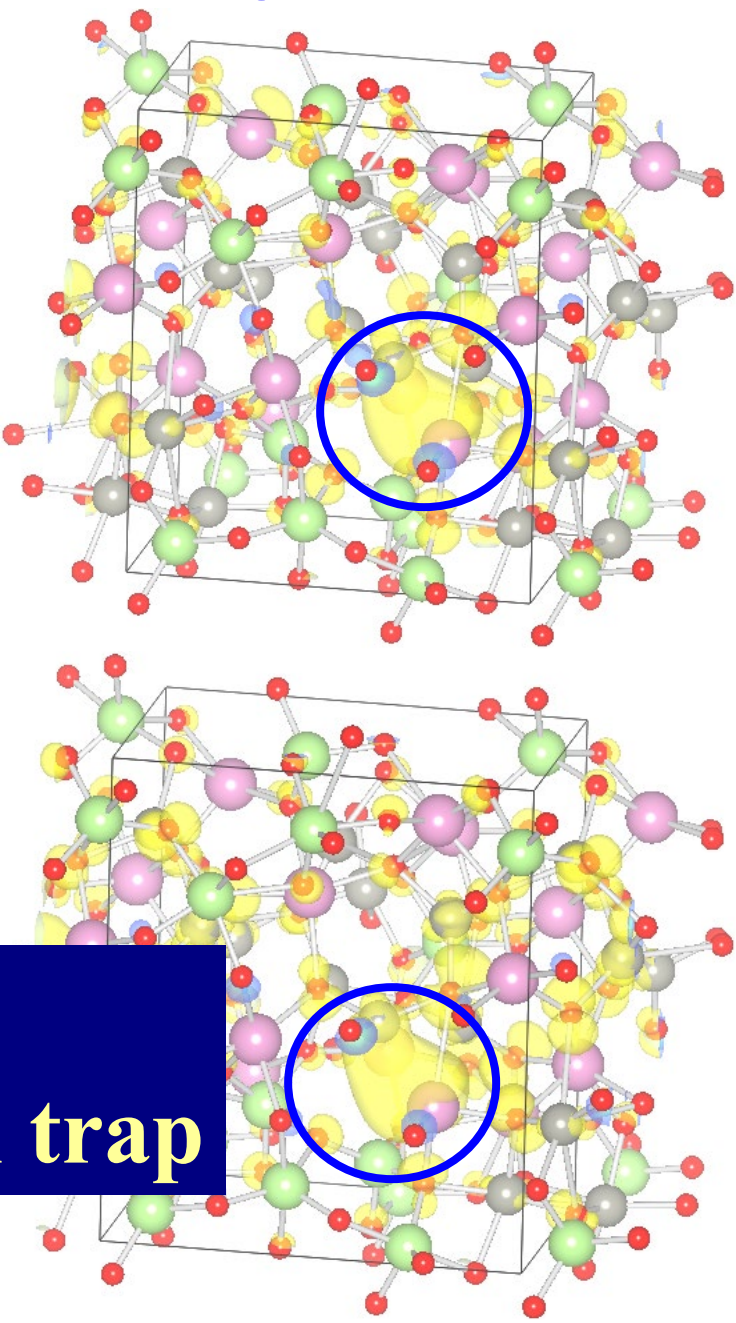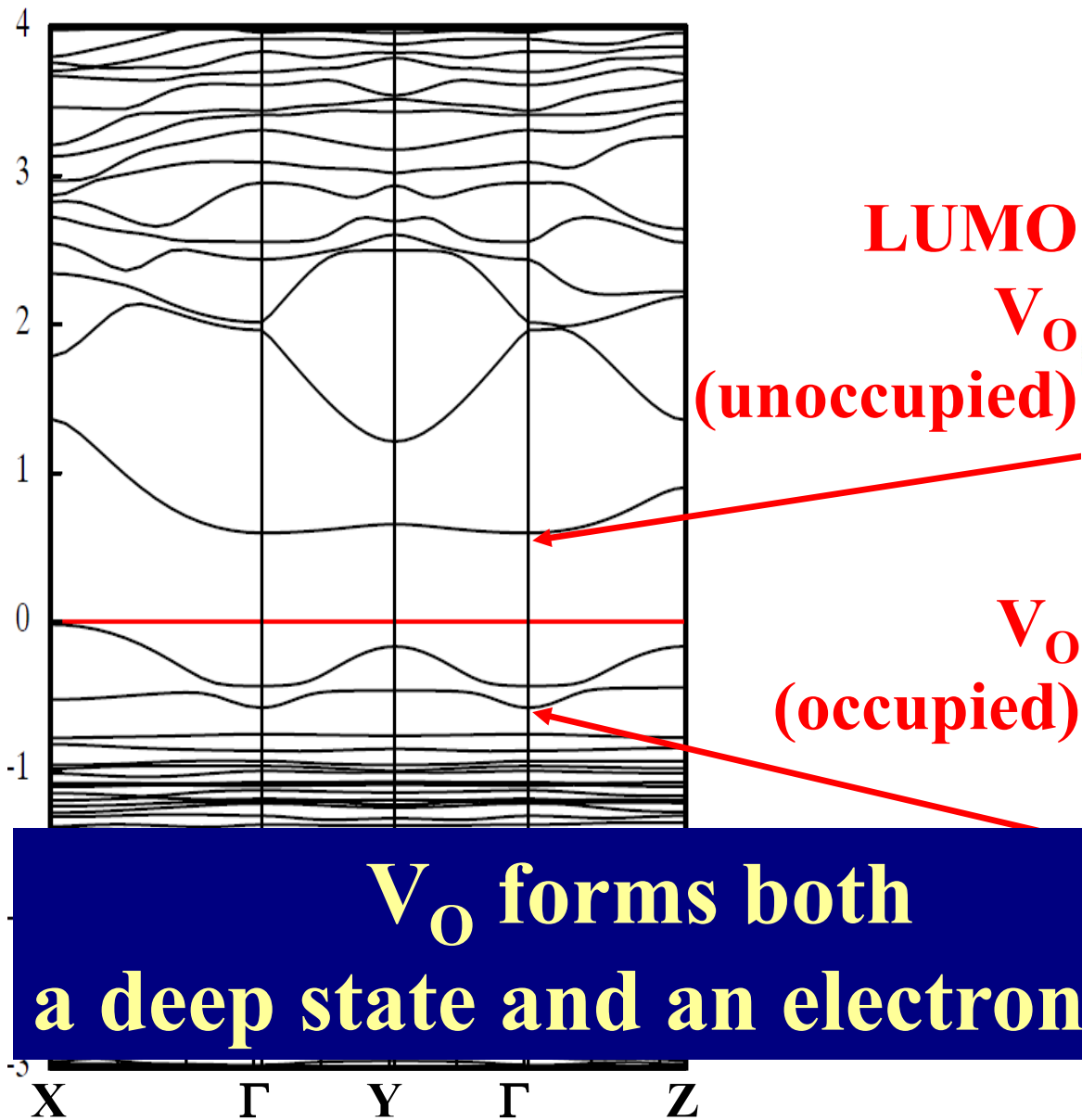
Origin of subgap states in amorphous In-Ga-Zn-O

Wolfgang Körner, Daniel F. Urban and Christian Elsässer
JAP 114, 163704 (2013).

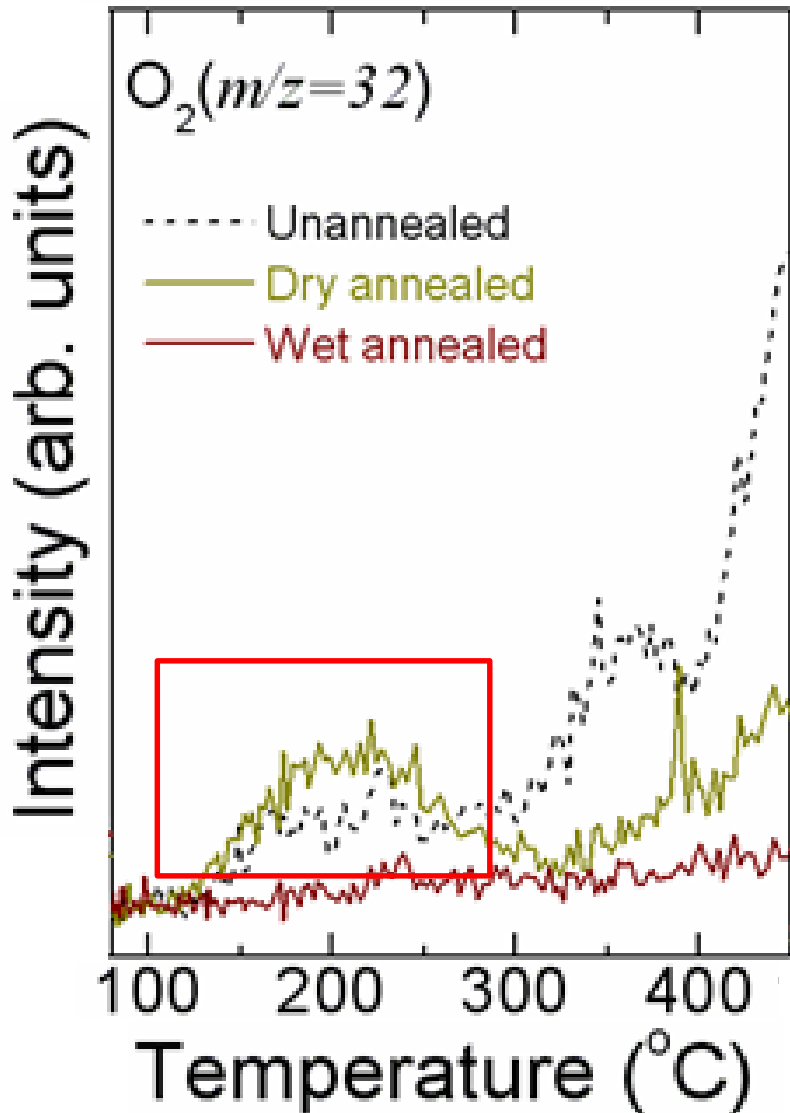**SIC: Self-interaction correction**

We present a density functional theory analysis of stoichiometric and nonstoichiometric, crystalline and amorphous In-Ga-Zn-O (c-IGZO, a-IGZO), which connects the recently experimentally discovered electronic subgap states to structural features of a-IGZO. In particular, we show that undercoordinated oxygen atoms create electronic defect levels in the lower half of the band gap up to about 1.5 eV above the valence band edge. As a second class of fundamental defects that appear in a-IGZO, we identify mainly pairs of metal atoms which are not separated by oxygen atoms in between. These defects cause electronic defect levels in the upper part of the band gap. Furthermore, we show that hydrogen doping can suppress the deep levels due to undercoordinated oxygen atoms while those of metal defects just undergo a shift within the band gap. Altogether our results provide an explanation for the experimentally observed effect that hydrogen doping increases the transparency and improves the conductivity of a-IGZO. © 2013

Origin of near-VBM states: Undercoordinated O

Effects of weakly-bonded O$_2$?

K. Nomura, Appl. Phys. Lett. **93**, 192107 (2008)

O$_2$(m/z=32)

----- Unannealed
——— Dry annealed
——— Wet annealed

Intensity (arb. units)

Temperature (°C)

As- and dry O$_2$ annelaed a-IGZO include weakly-bonded oxygen

Desorption amounts
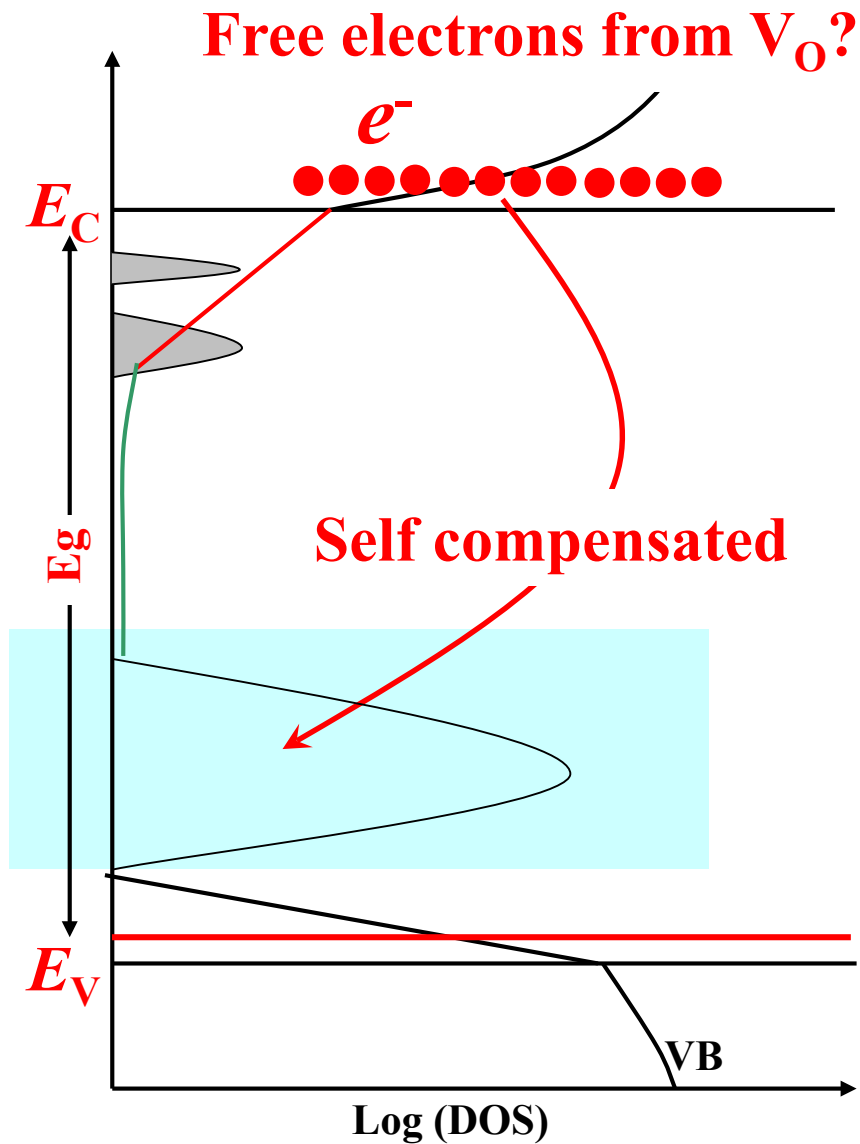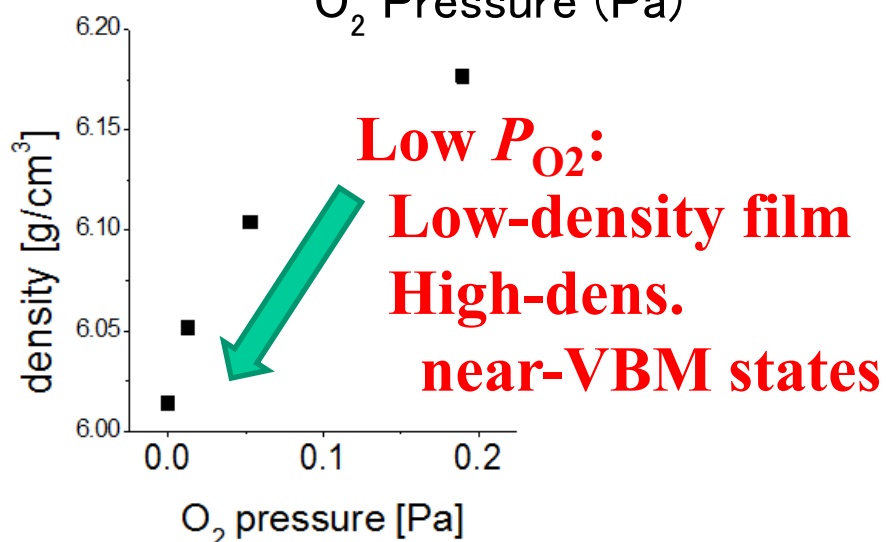**(×10^{18} cm^{-3}, up to 400°C)**
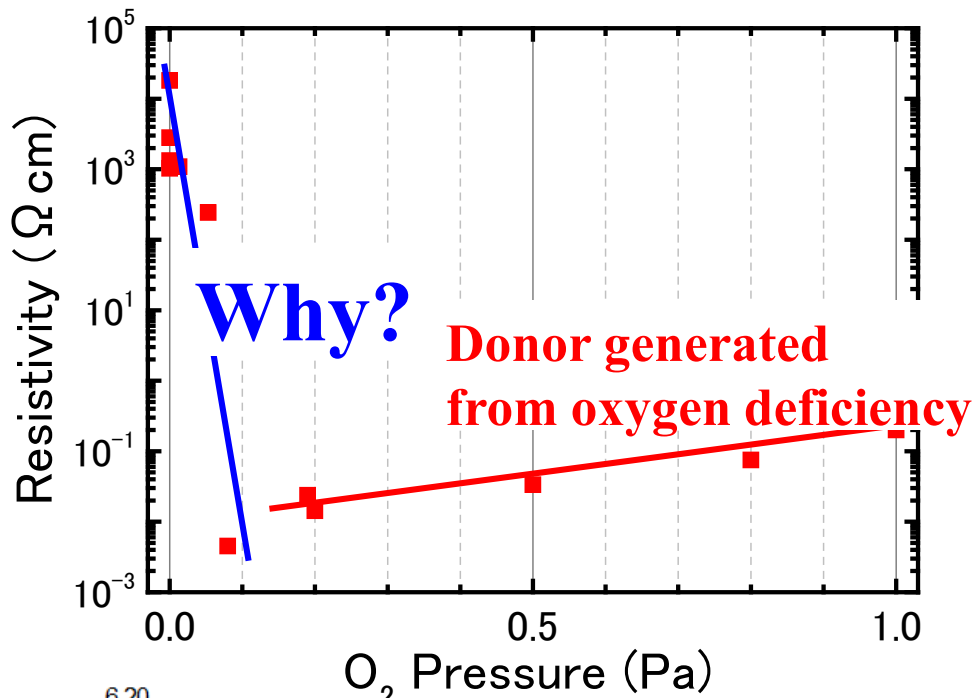**Unannealed   (~0.17)**
Dry O$_2$ (~0.11)

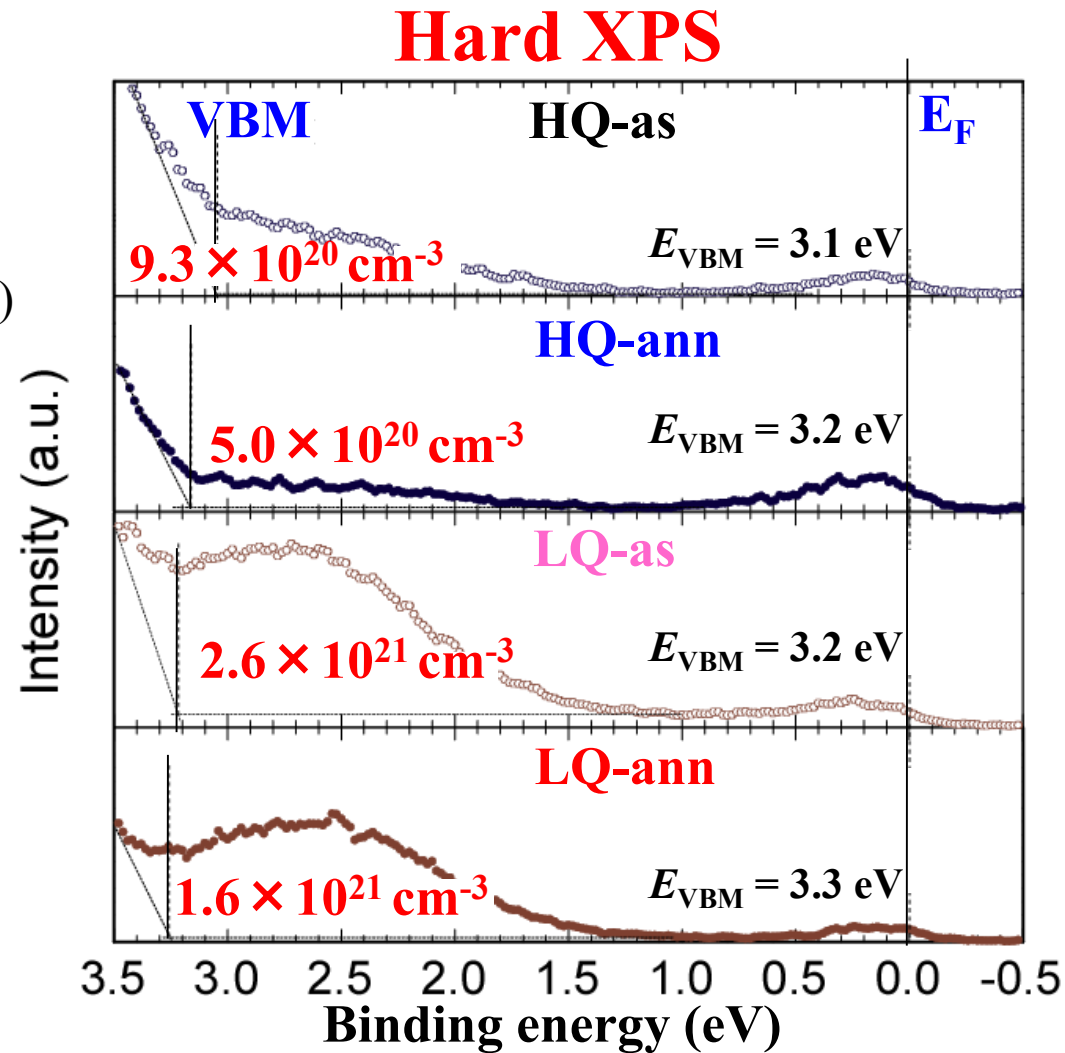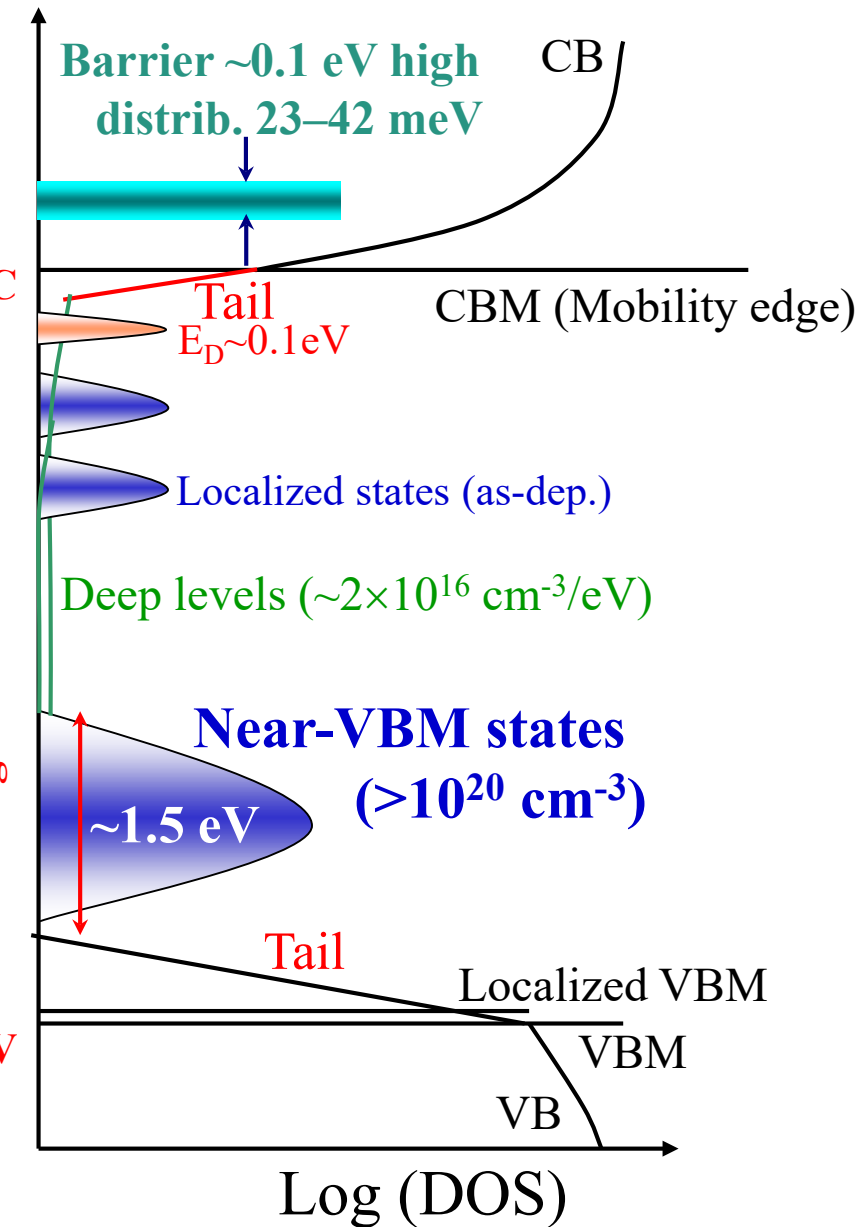**Wet annealing reduced them a lot Strong oxidation power?**

V_O model explains strong self-compensation in a-IGZO

By PLD @ low power

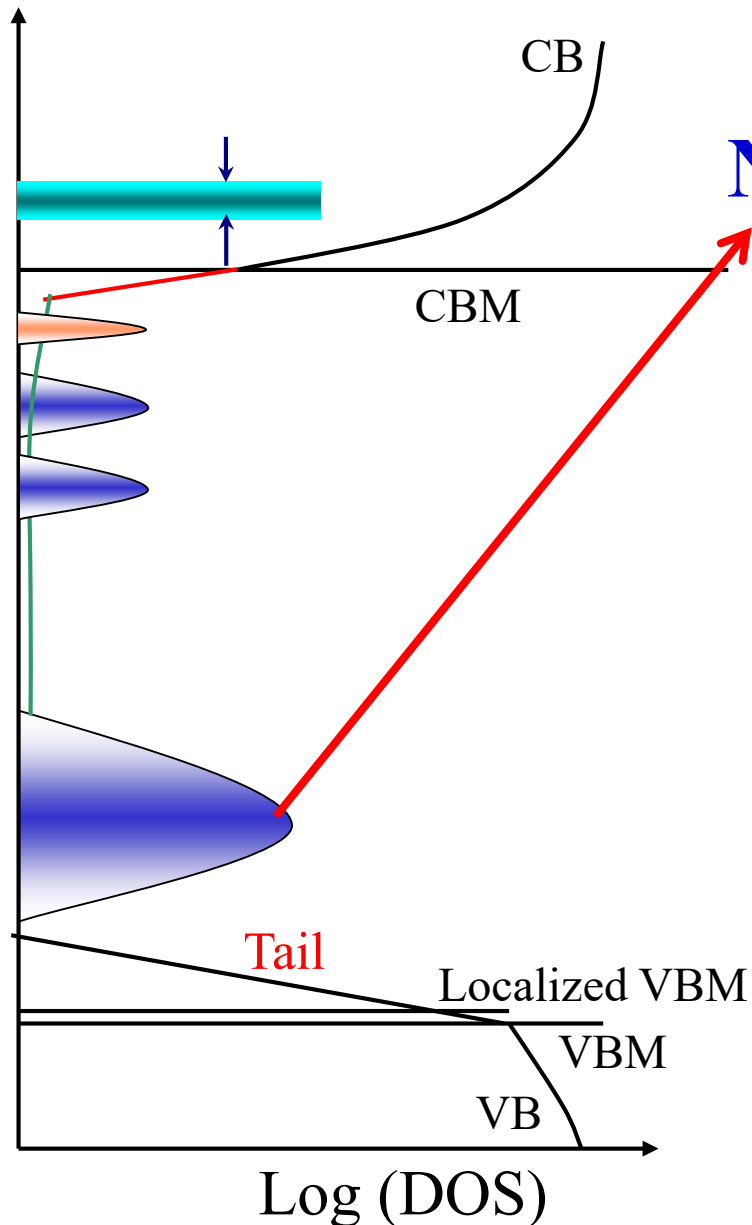ITC2014, Oxides9, J. Hermes, T. Orui et al.

Why?

Donor generated from oxygen deficiency

Free electrons from V_O?

e^-

E_C

Eg

Self compensated

E_V

VB

Log (DOS)

Low P_{O2}:
Low-density film
High-dens.
near-VBM states

Deep subgap states

Barrier ~0.1 eV high distrib. 23–42 meV

CB

Tail E_D~0.1eV

CBM (Mobility edge)

Localized states (as-dep.)

Deep levels (~2×10^{16} cm^{-3}/eV)

Near-VBM states (>10^{20} cm^{-3})

~1.5 eV

Tail

Localized VBM

VBM

VB

Log (DOS)

Hard XPS

VBM   HQ-as E_F

9.3×10^{20} cm^{-3} E_{VBM} = 3.1 eV

HQ-ann

5.0×10^{20} cm^{-3} E_{VBM} = 3.2 eV

LQ-as

2.6×10^{21} cm^{-3} E_{VBM} = 3.2 eV

LQ-ann

1.6×10^{21} cm^{-3} E_{VBM} = 3.3 eV

Intensity (a.u.)

Binding energy (eV)

3.5 3.0 2.5 2.0 1.5 1.0 0.5 0.0 -0.5

High-density defects exist above VBM

Proposed origins of near-VBM states

Near-VBM states

(i) V_o with void

Kamiya et a., pss(A) **207**, 1698 (2010)

(ii) Undercoordinated O

Körner et al., JAP **114**, 163704 (2013)

(iii) Weakly-bonded O^{n-}
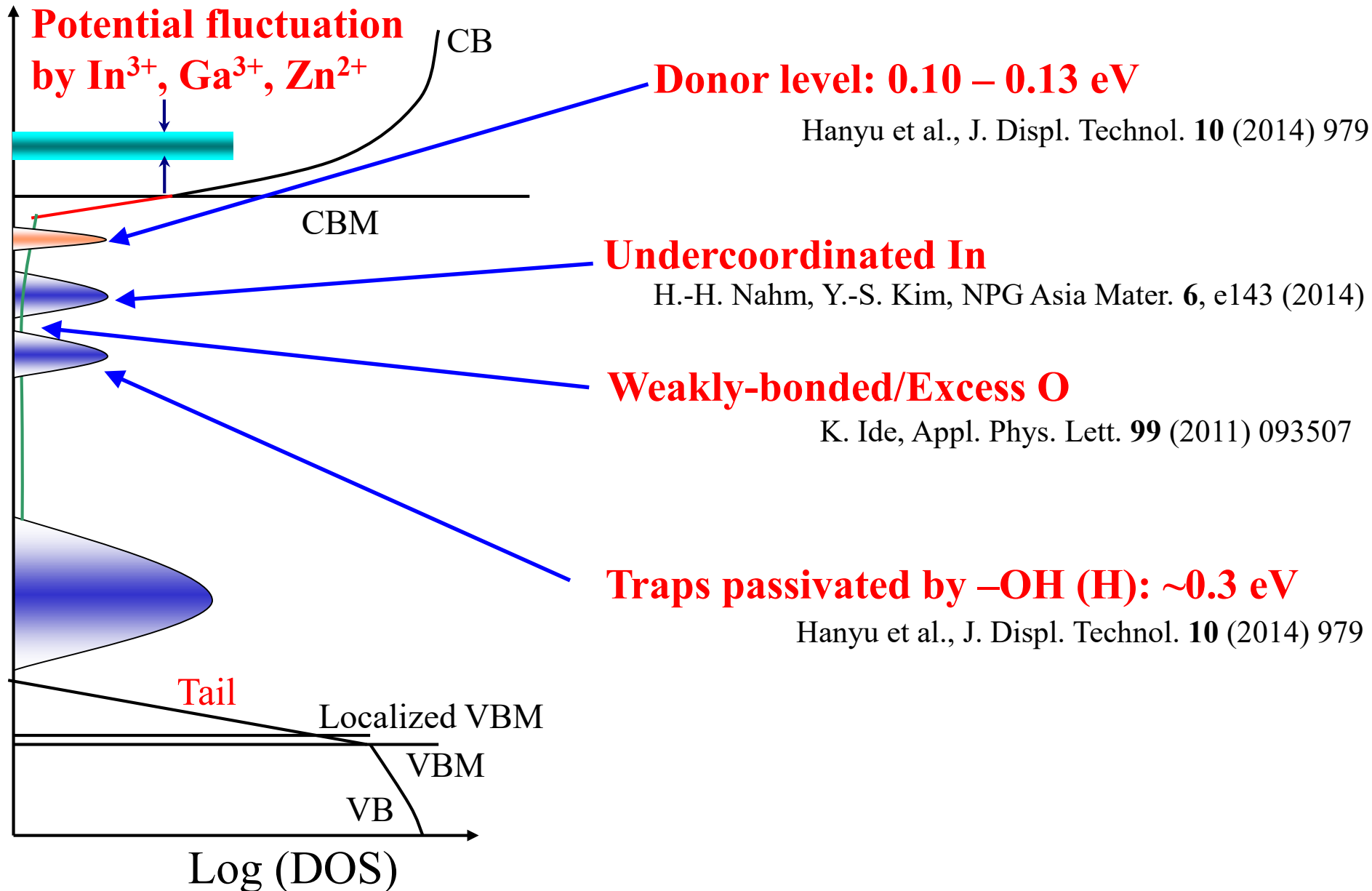
Ide et al., APL **99**, 093507 (2011)

(iv) –OH

Orui et al., JDT **11**, 518 (2015)
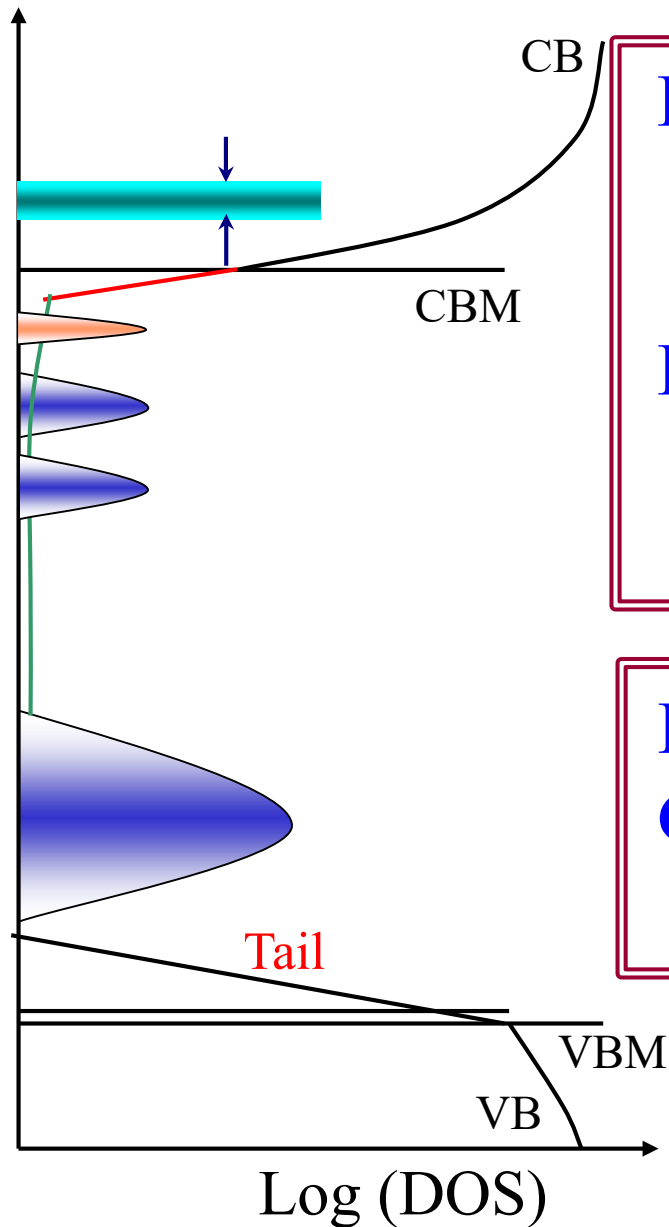
(v) H^{-}   **Bang et al., IDW2016**
December 9, 14:35   AMD7-4L

Hydrogen and subgap states in amorphous IGZO thin films

CB

CBM

Tail

Localized VBM

VBM

VB

Log (DOS)

Proposed origins of near-CB states

Potential fluctuation by In^{3+}, Ga^{3+}, Zn^{2+}

CB

CBM

Tail

Localized VBM

VBM

VB

Log (DOS)

Donor level: 0.10 – 0.13 eV

Hanyu et al., J. Displ. Technol. **10** (2014) 979

Undercoordinated In

H.-H. Nahm, Y.-S. Kim, NPG Asia Mater. **6**, e143 (2014)

Weakly-bonded/Excess O

K. Ide, Appl. Phys. Lett. **99** (2011) 093507

Traps passivated by –OH (H): ~0.3 eV

Hanyu et al., J. Displ. Technol. **10** (2014) 979

Why optimum R_{O2} window is narrow?

Low P_{O2}
V_O: donor, Near-VBM states
uc-O: Near-VBM states
High P_{O2}
Charged wb-/ex-O^{n-}: Near-VBM st.
uc-In: Shallow traps

Poor base pressure $>10^{-4}$ Pa: -OH, H^-
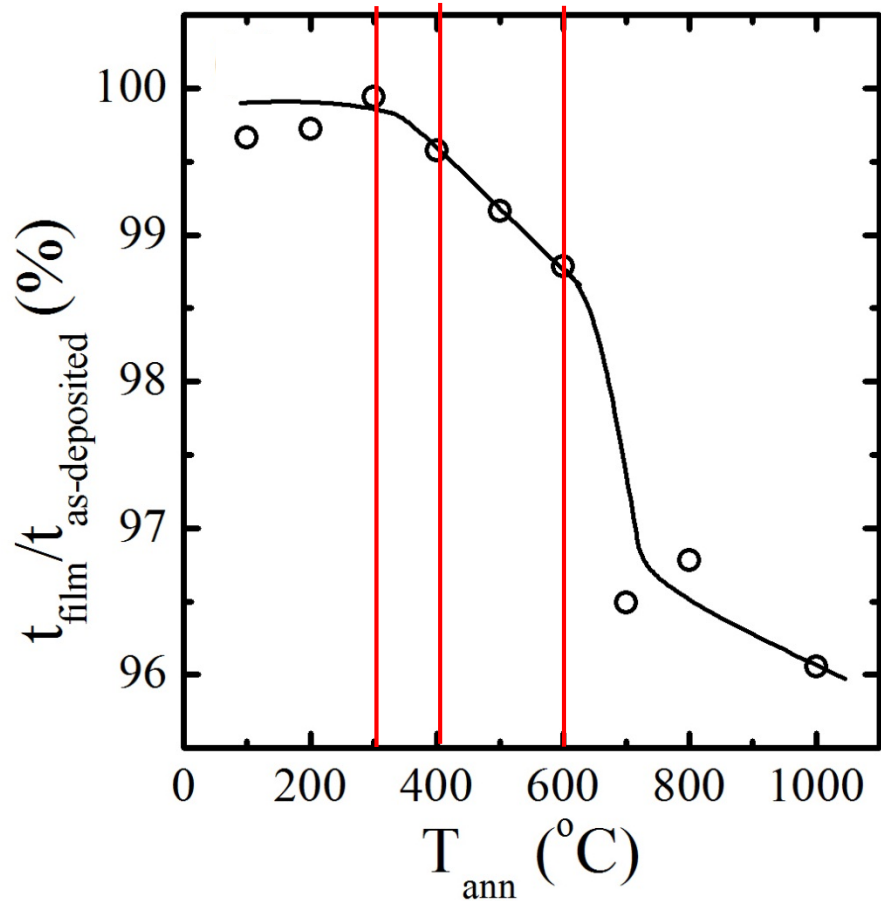**Good base pressure $\sim 10^{-7}$ Pa:**
Depassivation of deep traps

CB
CBM
Tail
VBM
VB
Log (DOS)

Deterioration by high-T (>400°C) anneailng
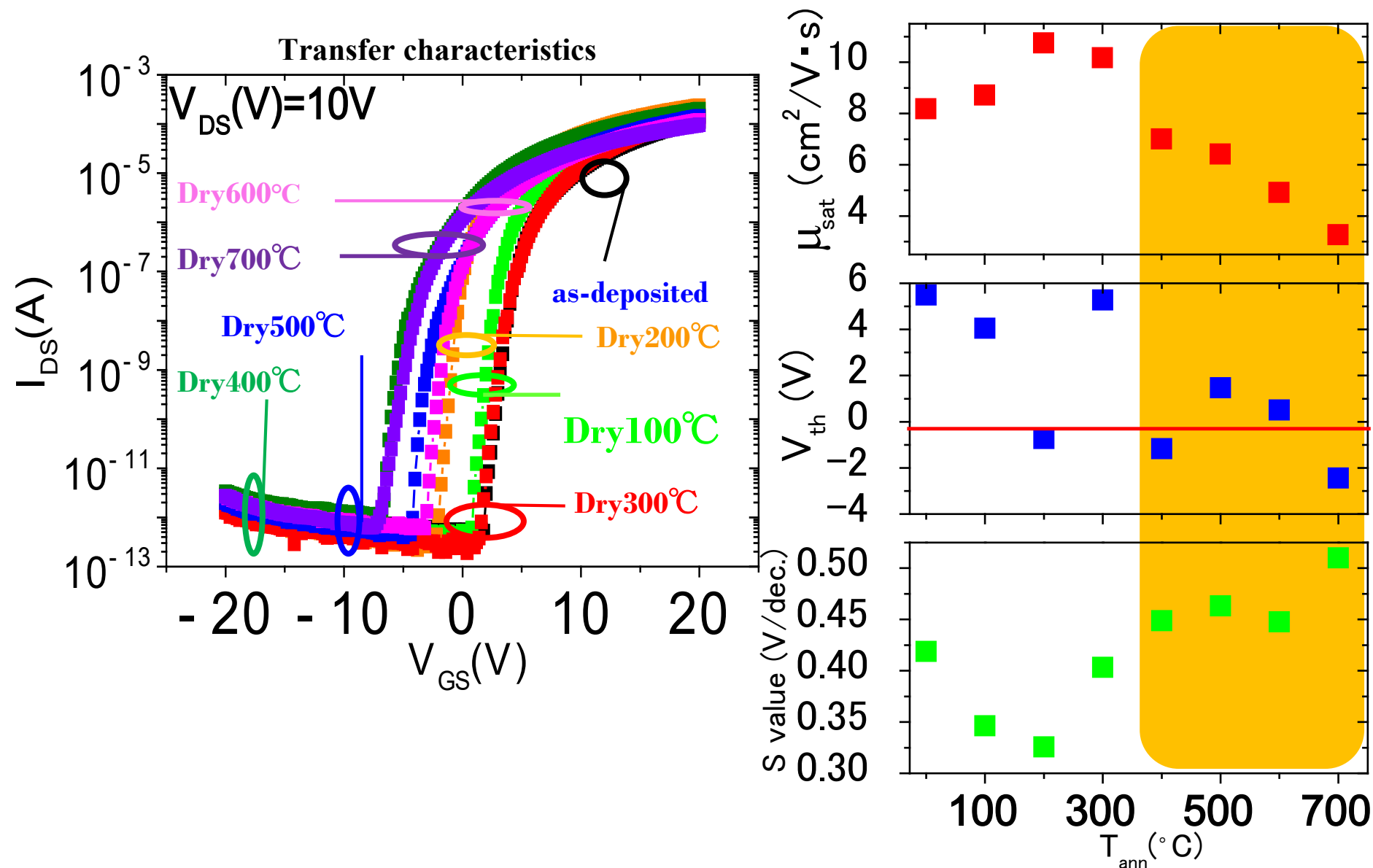
Densification and Eg change by annealing
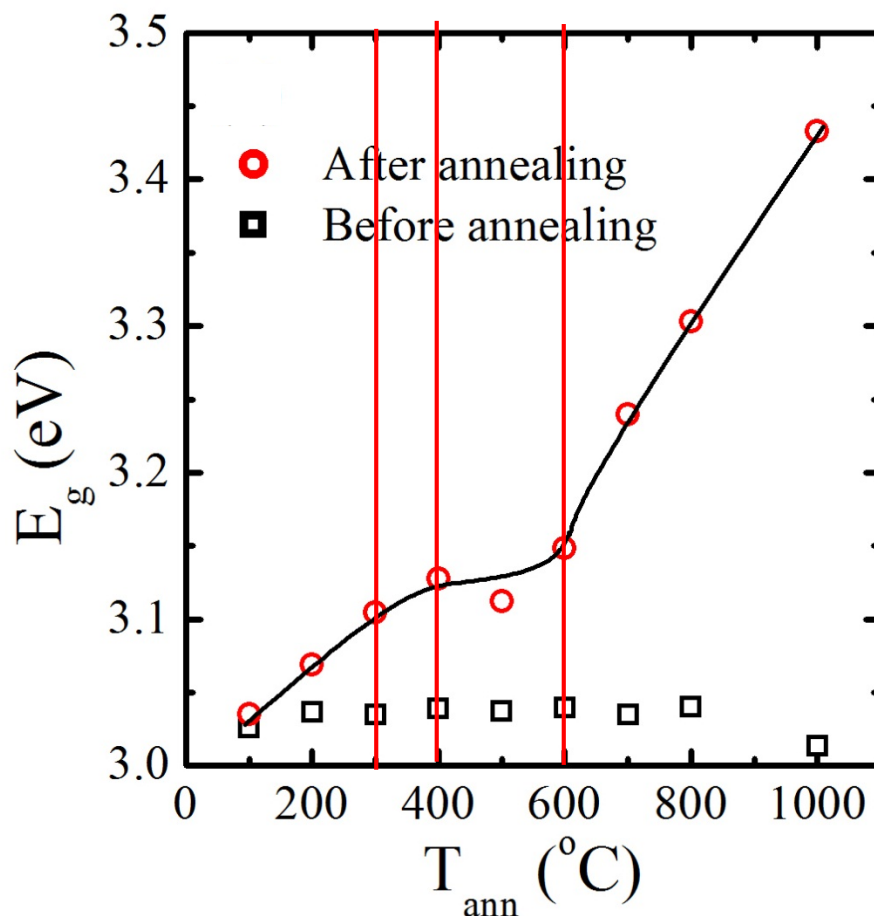
	Densification	E_g	Origin
<300°C	not detectable	increase	Tail state defect?
<400°C	Yes (0.3%)	increase	Network reconfiguration
<600°C	Yes (1.2%)	unchanged	
>600°C	Large (3.4%)	increase	Crystallization

Negative V_{th} shift by 200ºC annealing

Y. Hanyu et al., J. Displ. Technol. **10,** 979 (2014)
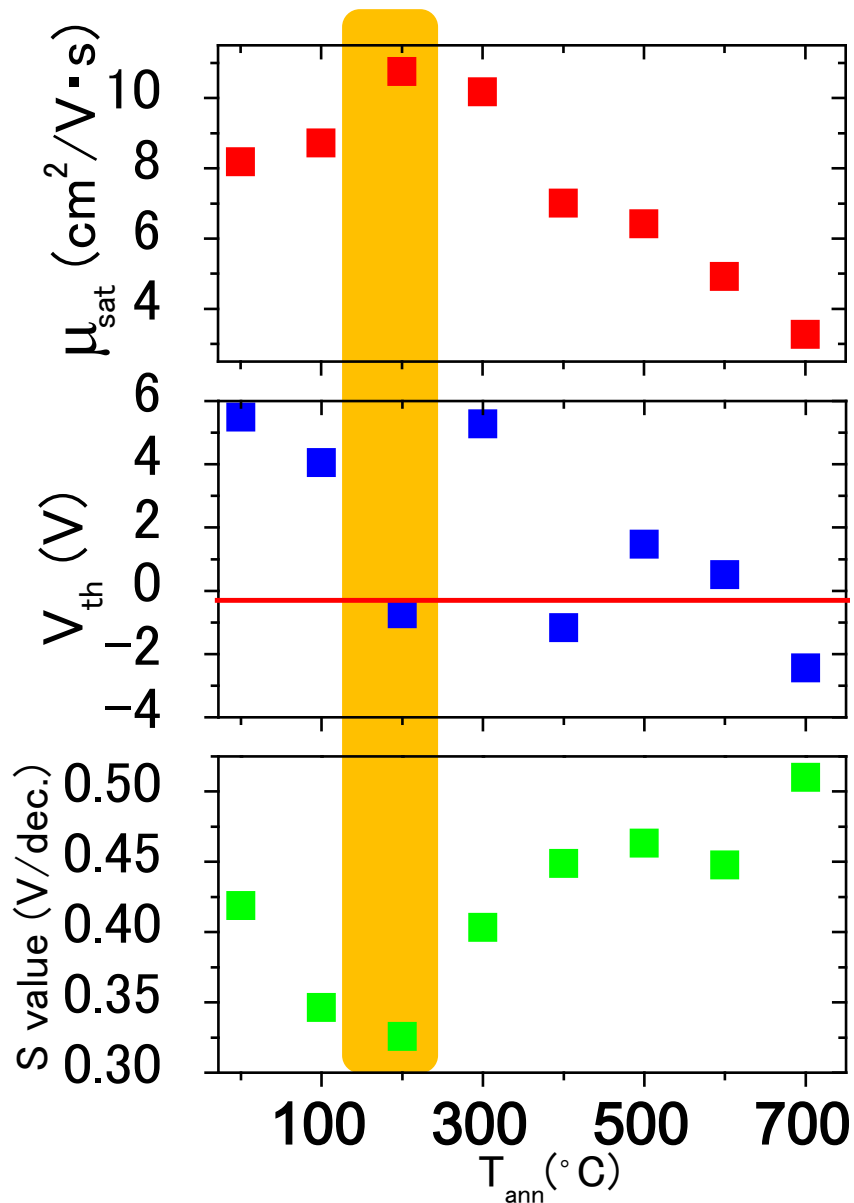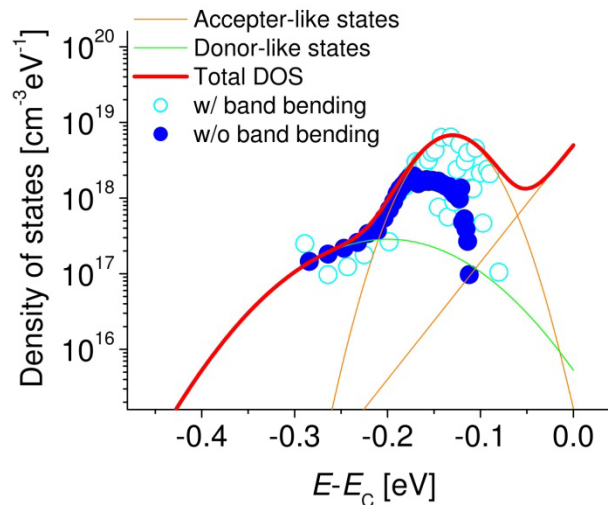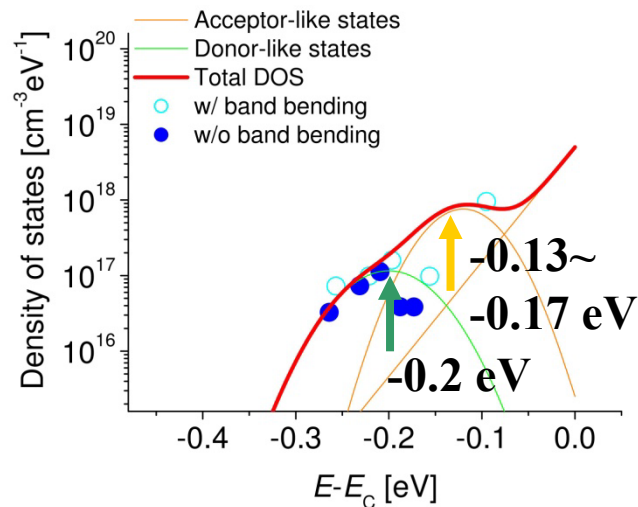
Slow relaxation: Stability

250°C annealing
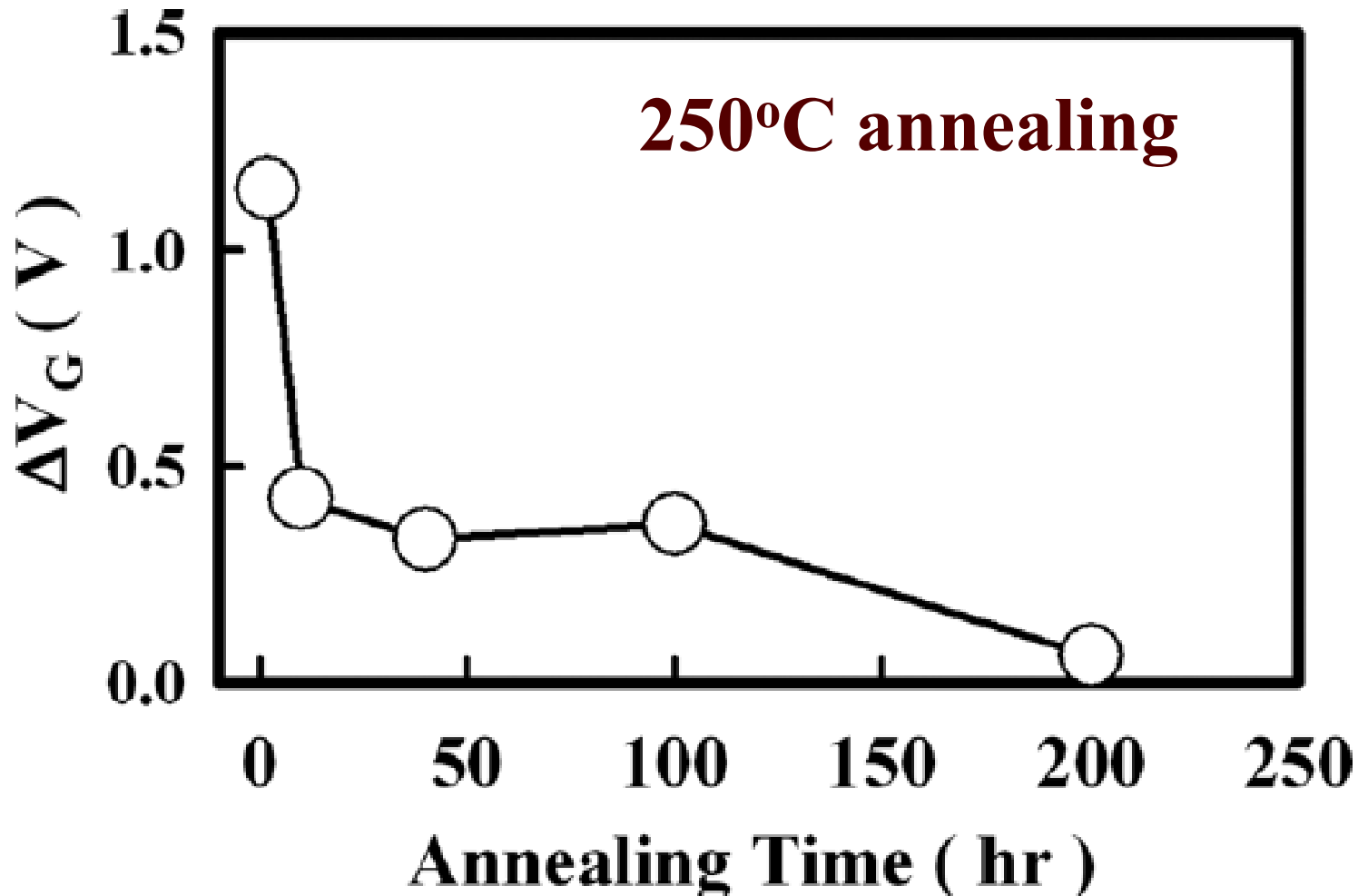
300ºC is necessary to oxidize a-IGZO

^{18}O analysis by SIMS
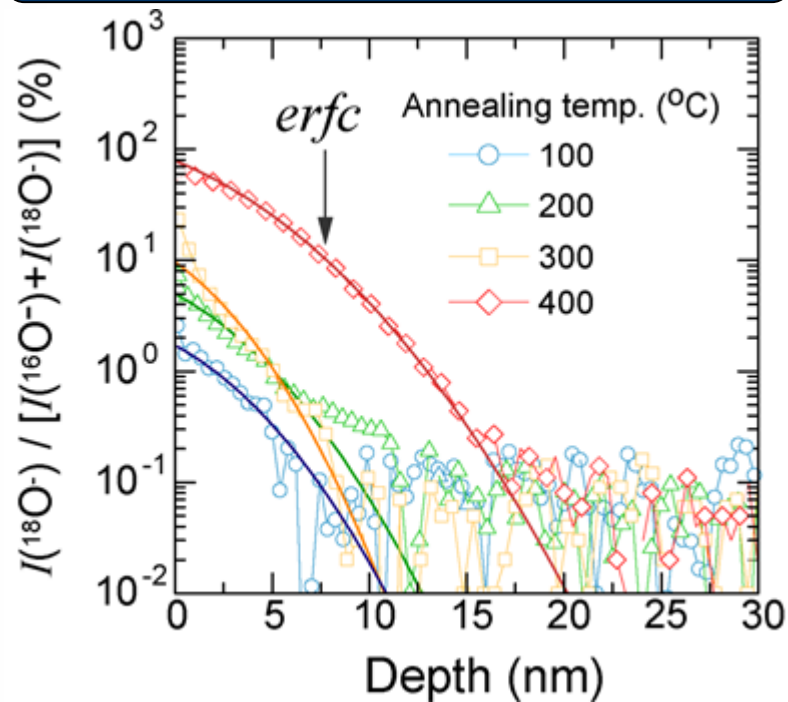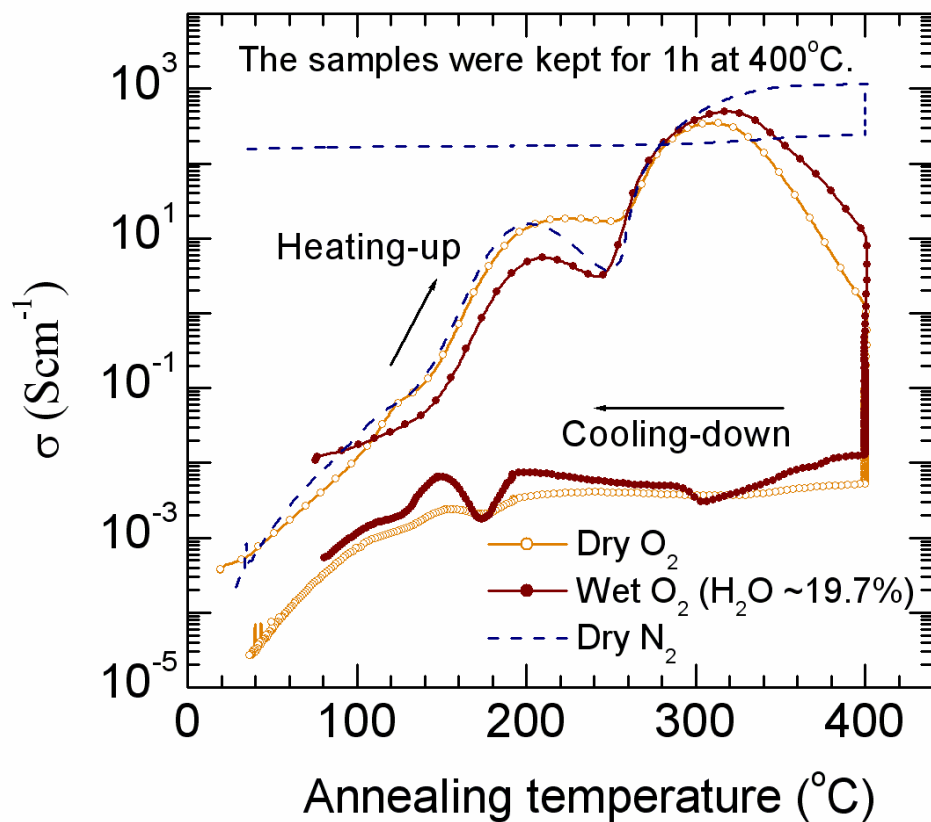
$D \sim 3 \times 10^{-17}$ cm^{2}s^{-1}@2-300ºC

Hydrogen diffusion in a-IGZO

K. Nomura, ECS JSS **2**, P5 (2013)
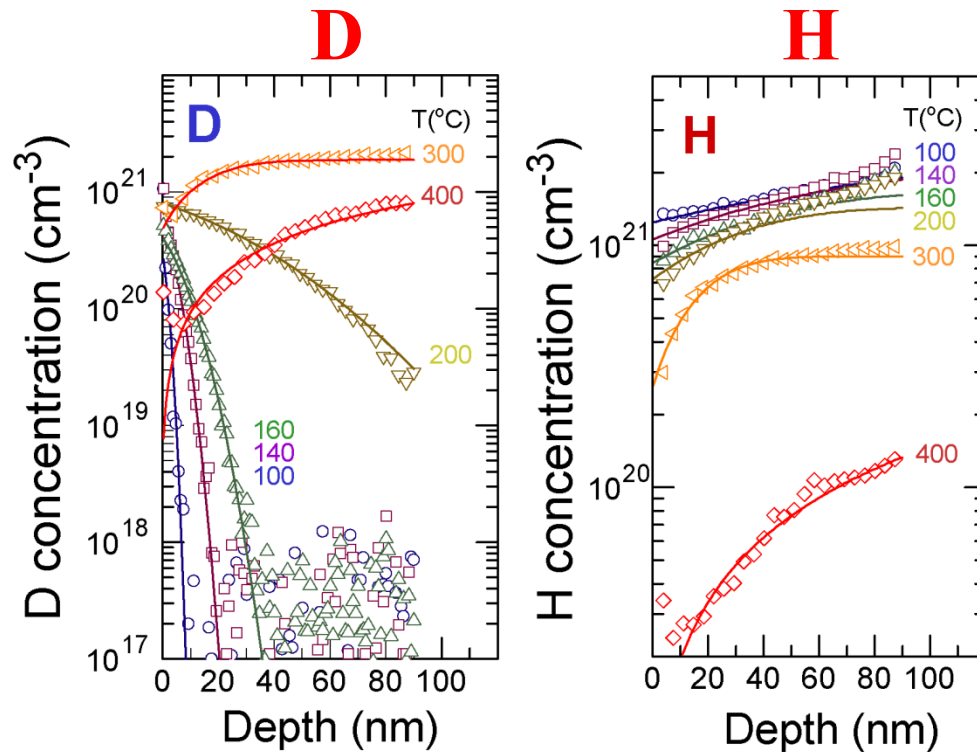
D   H E_a and C_0

$D \sim 10^{-15}$ cm^{2}s^{-1}@200°C
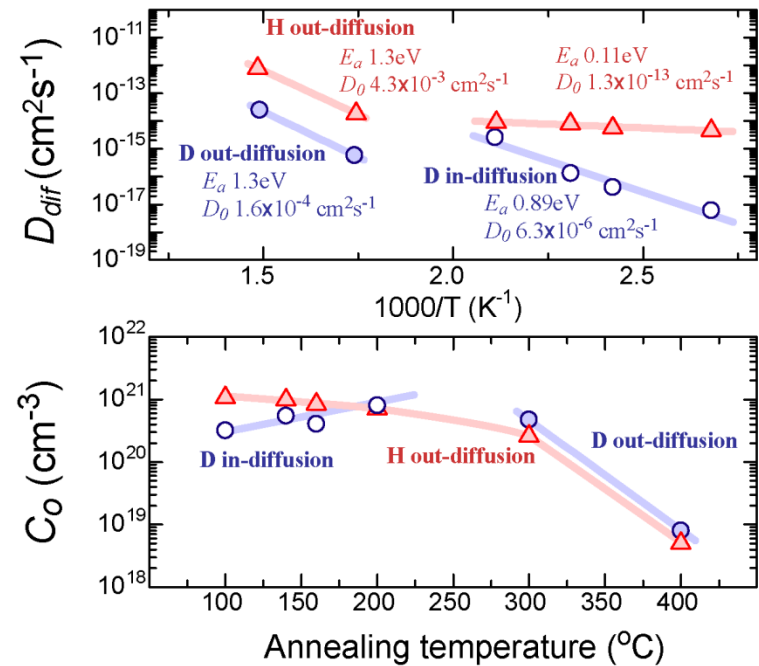
Cf. ZnO : ~10^{-10} @200°C
SiO$_2$: <10^{-6} @2000°C

Hole mobility ~ 0.01 cm^2/Vs
H mobility ~ 10^{-13} cm^2(Vs)$^{-1}$

Origin of negative V$_{th}$ shift by NBLS: Holes

In-situ high-T Hall measurement

t < 0 : **Raising T from room temperature**

t > 0から: **Keep temperature**
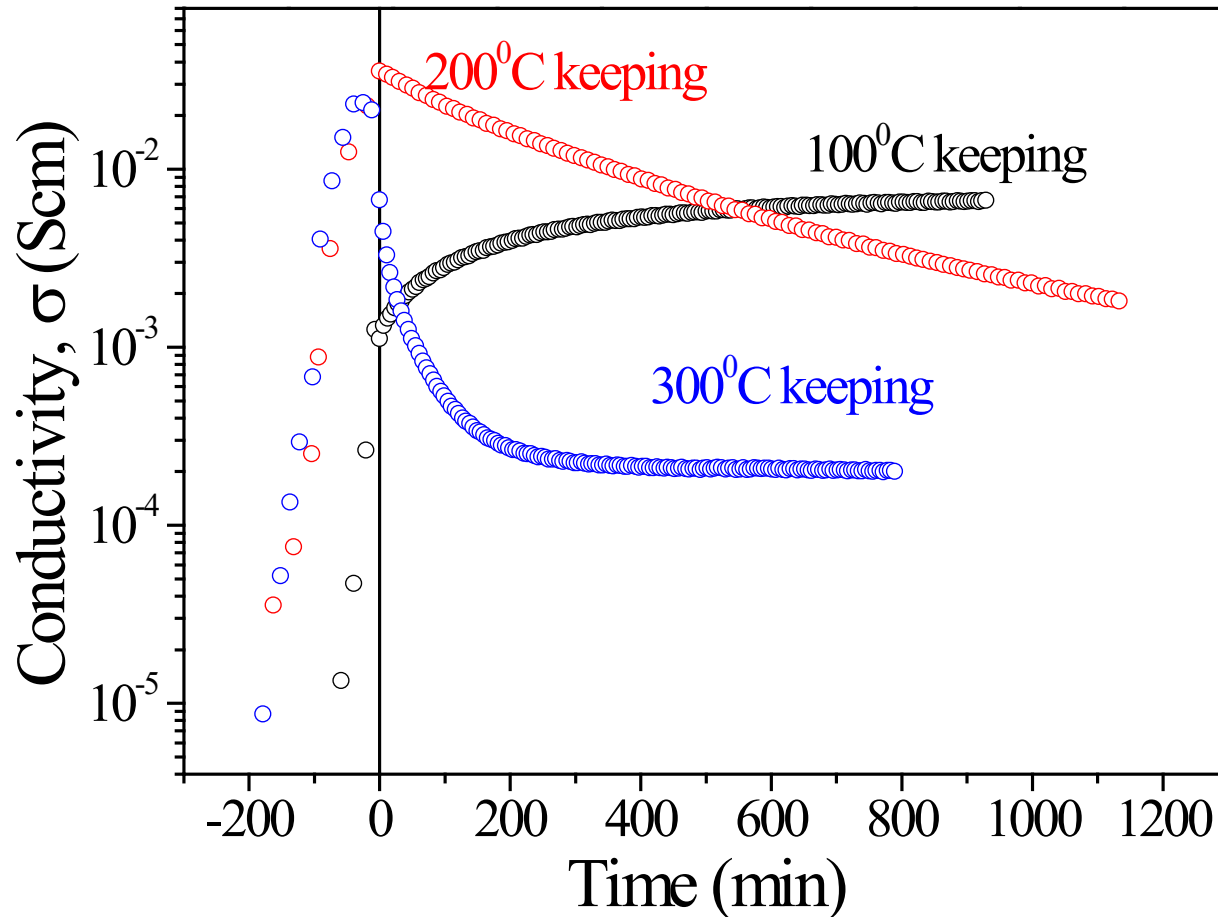
What happens at 400 – 500ºC?: Trap DOSs

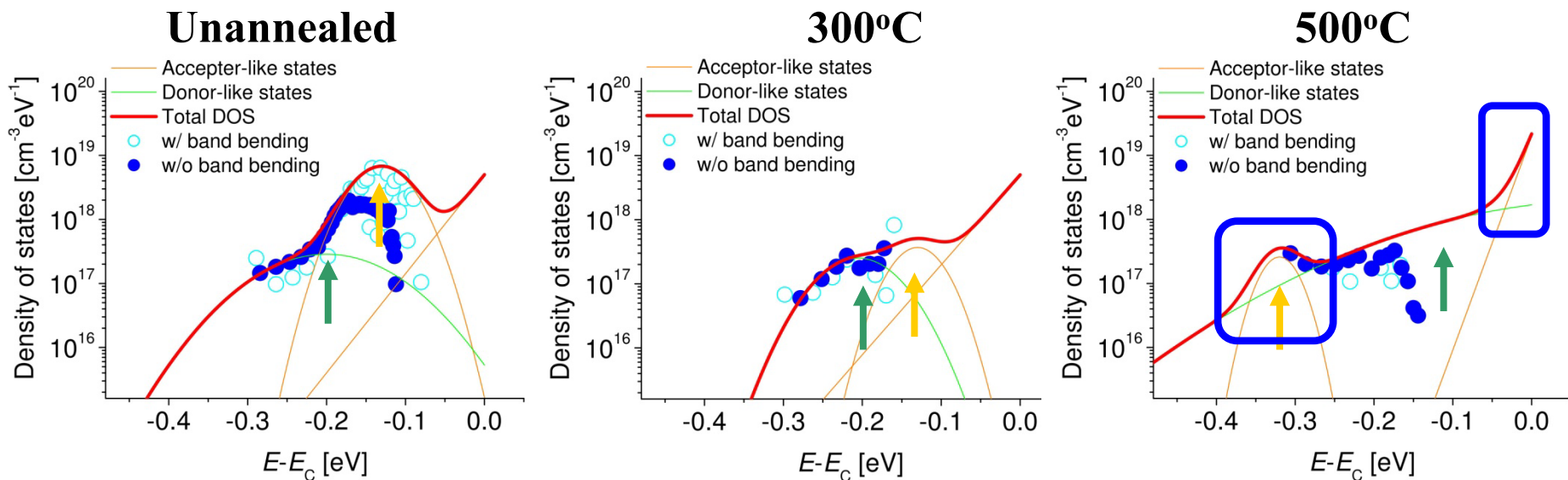Y. Hanyu et al., J. Displ. Technol. **10,** 979 (2014)

**500ºC annealing creates
deep traps and tail states**

Summary of hydrogen effects

	STD	UHV
[H]	$10^{20} \sim 10^{21}$ cm^{-3}	$<10^{19} \sim 4\times10^{19}$ cm^{-3}
Density (relaxation)	High (small)	Low (large)
Defect dens	Low	High
Conductivity	$>10^{-6}$ S/cm	$<10^{-8}$ S/cm
Desorption	Large (especially $300 - 500^{\circ}$C)	Hard to detect
Chem Comp	Zn-poor	Similar to target composition
After annealing		
Conductivity	Controllable to $\sim10^{-6}$ S/cm	
TFT	Good	Better than STD
TFT stability	△	×

Roles of hydrogen in a-IGZO：

- Enhance relaxation
  => Reduce deep traps
- Passivation some defects
- Easier E_F control

- H_2O desorption
  => Chem comp deviation
     Temperature instability
- Extra instability ($\Delta V_{th} \propto t^{1/4}$ law)